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Final Technical Report:

SOLID STATE IMAGE SENSOR RESEARCH

By W. E. Davern, R. E. Glusick, C. W. Kim,
M. E. Seymour and R. D. Stewart

March 1969

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Prepared under Contract No. NAS 12-131 by
GENERAL ELECTRIC COMPANY
Electronics Laboratory, Syracuse, New York
and
Missile and Space Division, Philadelphia, Pennsylvania

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
ELECTRONICS RESEARCH CENTER
CAMBRIDGE, MASSACHUSETTS

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General Electric Company
Syracuse, New York

ABSTRACT

50-element linear arrays of InAs photodiodes have been developed for radiation sensing in the 1-3 micron wavelength region. Monolithic fabrication techniques and controlled surface treatment have reduced leakage currents to 5×10^{-8} amps/cm^2. Device design, fabrication techniques, and optical and electrical measurements are described.

In addition, PbSnTe detectors were evaluated for application to 8-14 micron radiation sensing. This ternary compound offers a potentially higher operating temperature than doped Ge and a greater compositional uniformity than HgCdTe.

Read-out of the signal requires that high-sensitivity preamplifiers be used. Direct amplifications and charge-storage modes were evaluated for optimum system performance. A 50-channel amplifier-multiplexer was built.

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I. INTRODUCTION AND SUMMARY

The continuing development of meteorological satellite systems has placed heavy demands upon infrared sensor technology in terms of higher sensitivity, greater uniformity, higher operating temperature, and lower cost. These goals, coupled with the further requirement for array operation of the IR sensors, were the concern of the program "Solid State Image Sensor Research." This program, sponsored by NASA Electronics Research Center under contract NAS12-131, was carried out by the Electronics Laboratory of the General Electric Company, Syracuse, New York, and the Missile and Space Division of the General Electric Company, Philadelphia, Pennsylvania.

The program has consisted of three phases: a study program that evaluated detectors and their application to meteorological satellite systems over the 0.4 - 15 - micron band; a device and system development program during which an array of InAs detectors was first fabricated and placed in an electronically scanned readout system; and the present program that optimized the InAs detector array and the scanning circuits. In addition, one of the tasks of the second and third phases of the program was the study and evaluation of PbSnTe as a long-wavelength detector material.

The results of the Phase I study which led to the selection of the InAs array program are summarized below:

The visible region can be characterized by its advanced stage of device development, a high level of effort placed in array fabrication as a result of similarity to integrated circuit techniques, and a rather broad interest in applications. Several programs have been undertaken in this wavelength, although all are in the laboratory stage of development. The interest in the application is obviously high, since much of the information which is used in imaging systems lies in the visible. Interest is also spurred by the obvious commercial value of a solid-state image detector to the television industry.

The 2.5 to 5 micron region does not have the advantage of the device array fabrication techniques of the visible, although detector elements have been built and operated in small arrays. Some materials, particularly InAs and InSb can be grown with moderate uniformity. The amount of effort directed at producing an imaging system for this wavelength is quite small, however, and much effort can be expected before usable systems are available. The applications to meteorology appear to be some of the prime motivations for the use of this wavelength. Another important consideration is the ability to use scanning techniques quite similar to those developed or under development for the visible region. The one significant difference between the 2.5 - 5 micron region and the visible is the need for cooling. While not as severe as that required for 10 - 12 microns, the lower-temperature operation provides a definite limit on the choice of devices used in the scanning.

The 10 - 12 micron region is the least developed of all the regions from the point of view of materials, detectors, sensitivity, and scanning. The greatest reason for pursuing this wavelength is the long list of applications for 10 - 12 micron wavelengths. Whereas the other wavelengths require device or array work, basic material work is required for 10 - 12 microns. Cooling is also a rather severe limitation in that only active cooling apparatus will provide the 77^oK or lower temperatures required. The high interest in the meteorological applications, plus the new uses of 10.6 micron laser radiation detectors, have intensified the material and device work necessary to implement image sensors at this wavelength.

Details of the materials and detectors evaluated during the study phase of this contract appear in the "Phase I Technical Report, Solid-State Image Sensor Research," December 1966. The scanned InAs detector array is described in the "Phase II Technical Report, Solid-State Image Sensor Research," March 1968.

A. PROGRAM SUMMARY

InAs photovoltaic detectors are capable of providing background-limited detection for the 1 - 3 μ spectral region, while being cooled to only -80^oC. This capability, coupled with the ability to process monolithic arrays of detectors, provided the impetus to carry out the device optimization work of this contract. Uniformity and sensitivity were the primary goals.

Results demonstrate that the complex InAs material can be controlled to yield the desired device characteristics. A most important measure of this material control is the leakage current of the diode. State-of-the-art devices, prior to this present contract phase, exhibited leakage currents in the order of 10^{-3} - 10^{-6} amperes. Newly developed array devices now exhibit leakage current in the range of 10^{-9} - 10^{-12} amps. Fifty element arrays of such devices were fabricated and found to vary in responsivity by less than ±50 %.

It is now believed that the InAs array fabrication technology has been demonstrated such that the material may be reasonably considered for manufacturing methods programs which will provide the source of supply for space applications. Operated at 100^oK, the 0.005 × 0.007 inch detectors exhibit the following parameters:

$$\lambda_{max} = 3.1 \text{ microns}$$

$$\text{Responsivity} @ \lambda_{max} = 10^7 \text{ volts/watt}$$

$$D^* (\lambda_{max}, 500, 1) = 1.5 \times 10^{12} \text{ cm cps}^{\frac{1}{2}}/\text{watt}$$

Scanning circuits assembled during the second phase of the contract were designed to operate with the relatively low impedance devices then available. During this present phase of the program, high input impedence modifications were made to the circuitry, in order to maintain proper impedance matching with the detectors. In addition, completely new pre-amplifier circuits compatible with hybrid integrated assembly techniques were breadboarded and tested.

The most promising aspect of the improved devices is the capability of greatly reducing the complexity of the associated electronics. Direct charge-storage operation of the arrays was described during the study phase of the program, as the most desirable mode of operation. Its implementation, however, requires the use of high-impedance detectors, which were not available until the present effort. The primary advantage of the charge-storage mode is the capability of directly interrogating each detector in the array without the use of preamplifiers. For the eventual systems desired, this signifies a saving of several hundred amplifiers per system.

Another very significant implication of the low-leakage diode is the potential for fabricating a two-dimensional detector array using electron beam read-out, similar to the diode target vidicon tubes now being developed for visible use. Diode leakages of less than 5×10^{-8} amps/cm^2 are required, and were achieved, with silicon diode arrays, in order to generate T. V. format images. The leakage current density achieved with the diodes in the InAs array is 4.5×1^{-8} amps/cm^2 at -13 volts and 100^{o}K.

B. SOLID-STATE IMAGE SENSOR APPLICATIONS

As an example of a system utilizing arrays of the type being developed, consider an earth satellite with f/5 optics of 12-inch aperture.

For the three IR wavelength bands, 1.55 - 1.75, 2.2 - 2.4 and 10.5 - 12.5 microns, infrared detectors such as InAs and PbSnTe can be used to provide data at surface resolutions of 100 - 500 feet and thermal resolution of less than 1^{o}K. Photon levels from targets appear to be high enough compared with fluctuations in background levels, even when contrast is reduced by atmospheric scattering, that surface resolution should not suffer.

1. InAs

In the 1.55 - 1.75 and 2.2 - 2.4 micron bands InAs detectors can be used. InAs elements have been made as small as 0.005 inch and 0.002 inch appears feasible.

A signal to noise expression suitable for understanding the interrelationship of critical system parameters can be simply derived as follows:

$$V_s/V_n = KH/(NEPD) = K\theta^2 N \ t_o A_o/(NEP) \qquad (1)$$

$$= \pi K D \ t_o \ D^* \ \theta N/4 \ F\sqrt{\Delta f} \qquad (2)$$

where V_s/V_n is the peak signal to rms noise voltage ratio, H is the scene irradiance (w/cm^2) at the aperture, NEPD is the system noise limited noise-equivalent power density (w/cm^2).

K is the electronic degradation factor, which for any given pulse input is a function of the detector/noise filter combination, here = 0.5.

θ is angular resolution (radians)
N is scene radiance (w/cm^2 - sr)
t_o is optical transmittance, here = 0.5
A_o is optics collecting area (cm^2)
NEP is noise equivalent power (watts) - $FD\theta\sqrt{\Delta f}/D^*$
D is optical aperture - 30 cm for ERS
D* is normalized detectivity (cm $Hz^{\frac{1}{2}}w^{-1}$)
F is f/number = f/5 for typical design
and Δf is the electronic bandwidth (Hz) which is inversely proportional to dwell time.
$\Delta f = 1/2\pi t_D$

In order to achieve 100 foot nadir surface resolution from 500 nm altitude, θ must be 0.033 mr. In a 12-inch aperture f/5 system the detector element must be 0.005 cm on a side.

The D* values for InAs are about $1(10^{11})$ for 200^oK and $7(10^{11})$ for 77^oK at 2.3 microns and about 0.8 of these values at 1.65 microns. A temperature of 200^oK is achievable with passive radiative cooling only. The value of (V_s/V_n) calculated from (2) for a typical minimum radiance in the 1.55 - 1.75 micron band of $8(10^{-5})$ w/cm^2-sr is 6.1. For $5(10^{-5})w/cm^2$-sr in the 2.2 - 2.4 micron band, the value is 4.75.

This assumes a bandwidth of 1.6 KHz and dwell time of 10^{-4} second which corresponds to a system with 100 % efficient scan of 128 elements in a direction transverse to that of satellite motion.

$$t_d = (n/m)(s/V_s) = (128/6080)\left[100/3.47(6080)\right]$$

where n is number of detector elements
m is number of resolution elements across swath width of 100 nm
s is surface resolution
V_s is satellite suborbit velocity

Frame time for this scan is 12.8 msec.

For overlap with less efficient scan, n would increase. Scanning more rapidly would permit n to decrease, but would degrade sensitivity. The most sensitive system would have a pushbroom array of 6080 elements covering the entire swath width, maximizing the dwell time at (s/V_s) for n = m, at 4.74 msec, and increasing S/N by about 7 times over the system with 128 elements. Scanning a single detector element across the 6080 resolution elements does not appear feasible since this calls for dwell time of less than a microsecond.

The number of photons incident on a detector element during one exposure or dwell time is $Q = 8.3(10^{18}) N \theta^2 A_o t_o t_d$ at 1.65 microns

$$= 11.6(19^{18}) N \theta^2 A_o t_o t_d \text{ at 2.3 microns}$$

Target radiance at 30^o solar altitude and 1.55 - 1.75 microns is 1.29 w/m^2-sr and at 30^o and 2.2 - 2.4 microns is 0.658 w/m^2 - sr when modified by atmospheric scattering. This would provide $4.2(10^4)$ photons and $3.0(10^4)$ photons in these bands. These can be compared with fluctuations in background levels $Q_b^{\frac{1}{2}}$ of 158 photons and 156 photons in these bands. Since the ratios $Q_t/Q_b^{\frac{1}{2}}$ are over 200, resolution should not be degraded.

2. PbSnTe

In the 10.5 - 12.5 micron band PbSnTe is suggested as detector material because of its sensitivity at temperatures as high as 77°K, vs the 30°K needed for doped germanium detectors. A D* of $5(10^9)$ is believed possible.

Higher values of D* are achievable with photoconductive Ge:Hg, for example, with optics cooled to reduce the background photon flux Q_b: $D^* = \lambda_p/2hc\,(\eta/Q_b)^{\frac{1}{2}}$

where λ_p is wavelength of peak response = 14 microns

η = quantum efficiency factor = 0.16

If Q_b can be reduced below 10^{15} photons/cm^2-sec, D* of $5(10^{11})$ can be attained.

The sensitivity of a 10-micron infrared system is generally measured in terms of thermal resolution ΔT

$$\Delta T = NEP/\alpha\, T^3 p \theta^2 D^2 t_o$$

where α = Stefan-Boltzmann constant = $5.67\,(10^{-12})$ w/cm^2 deg^4

T = ambient temperature of surface = 285°K

p = fraction of surface radiation in spectral band = 0.125

and other terms are as defined earlier.

At long wavelengths, 100 foot resolution is not possible with 12-inch optics at 500 nm altitude. Considering the diffraction disk diameter limit of 0.1 milliradian, a 500-foot resolution (0.164 mr) is suggested. At f/2 this means 0.01 cm detector elements.

As for short wavelengths, maximum sensitivity is possible for a push-broom array of 1216 elements (ΔT = 0.064°K). However, with only 12 elements (100 % efficient scan) T = 0.64°K, which should provide acceptable sensitivity. Frame time is then 0.29 sec and dwell time is 0.237 msec, which is significantly longer than detector response time.

The number of photons incident on a detector element during one dwell time is $Q = 58\,(10^{18})\, N\theta^2\, A_o t_o t_d$ at 11.5 microns.

Target radiance as modified by the atmosphere is 11.66 w/m^2-sr vs 11.02 w/m^2-sr for background differing by 5°K. Target photons per dwell time then number about $1.56\,(10^8)$ and fluctuation in background photons about $1.21\,(10^4)$ providing a ratio $Q_t/Q_b^{\frac{1}{2}}$ of over 10^4. Resolution here should not be degraded. Note that even for smaller ΔT such as 1°K, this ratio does not change significantly.

3. Summary

Characteristics of infrared scanning sensors in a 12-inch aperture system with 0.5 optical efficiency operating at 500 nm altitude are summarized in Table I.

TABLE I. SUMMARY OF SENSOR CHARACTERISTICS

Spectral Range $\Delta\lambda$ (μ)	1.55 - 1.75	2.2 - 2.4	10.5 - 12.5
Optical Relative Aperture	f/5	f/5	f/2
Nadir Surface Resolution S (ft)	100	100	500
Angular Resolution θ (mr)	0.033	0.033	0.164
Detector Type	InAs	InAs	PbSnTe
Detector Size (cm)	0.005	0.005	0.01
Detectivity D* (cm $Hz^{\frac{1}{2}}w^{-1}$)	8 (10^{10})	1 (10^{11})	5(10^9)
Operating Temperature	200^{o}K	200^{o}K	77^{o}K
Number of Elements (100 % eff. scan)	128	128	12
Dwell Time (microseconds)	100	100	237
Frame Time (milliseconds)	12.8	12.8	290
Scene Signal/System noise at 30^o solar altitude	6.1	4.75	---
Thermal Resolution	---	---	0.64^{o}K

II. InAs PHOTODETECTOR DEVELOPMENT

A. THEORETICAL CONSIDERATION OF PHOTODETECTORS

1. Introduction

The principle of operation of the p-n junction diode as a photodetector is quite simple. When the incident photons whose energy is greater than the bandgap of the semiconductor are absorbed on a p-n junction diode, electron-hole pairs are generated in the junction. The minority carriers generated within a diffusion length will diffuse toward the junction where they come under the influence of the built-in electric field and are separated. This separation produces a measurable electrical signal between the p and n regions. If the p and n contacts are shorted, a short-circuit current can be measured; if the p and n contact leads are opened, an open-circuit voltage will appear at the output. This output voltage is called a photovoltage, and this type of operation of p-n junction diode is called the photovoltaic mode of operation.

A p-n junction diode can also be used as a photodetector with a reverse-bias voltage to the diode. A diode used in this way is known as a photodiode. When a p-n junction photodiode is biased in the reverse direction, it exhibits a very high resistance and small constant saturation current; the device operates as a photoconductor. From the junction theory, the reverse saturation current carried by one type of minority carrier is proportional to the density of this carrier, so that, if the minority carrier density is increased by light, the saturation current will also be increased. Thus, the current increase will be proportional to the incident light intensity.

The photovoltaic detector has the advantage that no external voltage supply is required. The photovoltage comes about from the reduction of the potential barrier at the junction by the photo-generated carriers. Therefore, the photovoltaic detector can be regarded as a transducer which converts radiant energy into an electrical potential. However, the output photovoltage is not directly proportional to the intensity of the incident light over a large range of light intensity. Only for low illumination levels will linear operation be possible, as seen later in the experimental results.

It has been shown in a previous report[1] that in order for the photovoltaic diode to be operated in the linear region, the intensity level must be low enough so that the open-circuit voltage of the diode is much less than kT/q. When the intensity of the incident radiation is high, the generated voltage will rise slowly until it removes the barrier of the junction, when no further increase can be expected. The maximum photovoltage which can be generated for each photovoltaic p-n junction diode is thus equal to that obtained from the difference in the Fermi levels of the p-type and n-type material at the junction.

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[1] Phase II Report. Solid State Image Sensor Research (NAS 12-131).

The experimental results will show this later in this report.

The major application of the photodetectors, particularly in the infrared region, is in the low radiation level and therefore,the sensitivity of the detector is very important. The sensitivity is usually limited by the device noise and is, in fact,expressed in terms of the noise-equivalent power of the detector. The primary sources of noise are (1) Johnson noise, (2) shot noise, and (3) background noise. The background noise, in general, is **smaller** than either the Johnson or shot noise.

The sensitivity of a reverse-biased photodiode is limited by the shot and Johnson noise, which are a result of the reverse saturation current and the load resistance in the biasing circuit, respectively; whereas the sensitivity of a photovoltaic diode is limited only by the Johnson noise which results from the dynamic resistance of the diode at the zero basis.

A theoretical analysis of the photovoltaic InAs photodetector is presented, in some detail, in Section II. A. 2., following. The results are given in graphical form, by means of a computer. The analysis was prompted by the need for practical design criteria for obtaining optimum junction depth with given material and device parameters.

2. Theoretical Analysis of a Photovoltaic Diode

The sensitivity of the photovoltaic signal depends on the many device parameters and on charge transport mechanisms. If the charge carriers are generated in a nondepletion region, they are transported by diffusion to the depletion region of the diode. During the process, carrier recombination also takes place due to a finite minority carrier lifetime. Only those charges diffused to the junction contribute to the signal. Therefore, the sensitivity depends upon this ability of the minority carriers to diffuse to the junction. The diffusion ability of the carriers is described by the diffusion length, which is determined by the mobility and lifetime. A longer diffusion length means less recombination of the carriers, leading to a higher sensitivity.

The sensitivity also depends on the surface recombination velocity, since the carriers generated near the surface readily recombine at the surface. This effect is increased when the incident radiation has a high absorption coefficient. Thus, to increase the sensitivity it is necessary to decrease the surface recombination velocity.

Therefore, the sensitivity is a function of the carrier diffusion length, the junction depth, the surface recombination velocity, and the absorption constant of the material at the incident radiation wavelength. An analytical expression of the output signal voltage of a photovoltaic photodetector was derived in the Phase II report and the result is given as:

$$V = \frac{\alpha\tau_e\left\{L_e(\alpha D_e+S)-\left[D_e\sinh x_o+SL_e\cosh x_o+\alpha L_e(SL_e\sinh x_o+D_e\cosh x_o)\right]e^{-\alpha x_j}\right\}}{\beta(\alpha^2L_e^2-1)\left\{n_o(SL_e\cosh x_o+D_e\sinh x_o)+\dfrac{p_oL_eD_h(SL_e\sinh x_o+D_e\cosh x_o)}{L_hD_e\tanh\dfrac{(x_t-x_j)}{L_h}}\right\}}N$$

where

α	is the absorption coefficient
S	is the surface recombination velocity
N	is the number of photons/cm^2sec
p_oN_o	are the equilibrium carrier densities
L_eL_h	are the minority carrier diffusion lengths
D_eD_h	are the minority carrier diffusion control
β =	q/kT
x_t	is the sample thickness
x_g	is the junction depth
x_o =	x_j/L_e

To compute the above equation, the following data for InAs were used:

Operating temperature, T	=	200^oK
Wavelength, λ	=	$3.3\ \mu$
Absorption coefficient, α	=	$2 \times 10^3\ cm^{-1}$
Electron mobility, μ_e	=	14,000 cm^2/volt-sec
Junction area, A	=	$1.94 \times 10^{-4}\ cm^2$
p_o	=	$10^{10}\ cm^{-3}$
n_o	=	$10^{11}\ cm^{-3}$
$\frac{\tau_e}{\tau_h}$	=	10
$x_t - x_j$	$\gg$	L_h
x_t	=	3×10^{-2} cm

a. Responsivity

With the above assumed values, the photovoltaic responsivity defined as the signal voltage per unit optical power (volts/watt) has been computed for the different values of lifetime (τ_e) and surface recombination velocity(s) as a function of the junction depth (x_j).

The analysis is used to find an optimum junction depth when the material and device parameters are given. Since some of the parameters such as the lifetime and surface recombination velocity are not certain, different sets of values were used to determine the optimum junction depths. With these optimum junction depths, the effect of device performance on the device parameters is studied, and the results are qualitatively compared with the experimental results.

The results of the responsivity calculations are shown in Figures 1 and 2. These figures show the responsivity versus the junction depth, x_j, with the lifetime, τ_e, as a running parameter for given values of surface recombination velocity, S. The values of S are 10^3 cm/sec and 10^5 cm/sec for each figure, respectively. It is evident that a low value of lifetime seriously affects the shape of the curves at large values of x_j and the optimum junction depths are decreased with the lifetimes. This is due to the inability of the carriers to diffuse to the deep junctions for the low lifetime. But for high lifetime, the curves become plateaus after reaching the peaks. These results are summarized in Table II.

TABLE II. SUMMARY OF RESPONSIVITY CALCULATION RESULTS

S(cm/s)	τ_e(sec)	$L_e(\mu)$	$x_{jo}(\mu)$	Peak Responsivity (volts/watt)
10^3	10^{-5}	490	23.5	2.38×10^6
	10^{-6}	155	18	7.8×10^5
	10^{-7}	49	12	2.13×10^5
	10^{-8}	15.5	8	4.67×10^4
10^5	10^{-5}	490	26	1.6×10^5
	10^{-6}	155	20	1.3×10^5
	10^{-7}	49	14	1.3×10^5
	10^{-8}	15.5	8	3.2×10^4

It is interesting to note that the effect of an increase in the lifetime or diffusion length is to shift the optimum junction depth to larger values, and that the effect of an increase in the surface recombination velocity is, similarly, to shift the optimum junction depth to larger values. Note that no appreciable changes result from further decreases in the surface recombination velocity below 10^3 cm/s.

In Figures 1 and 2, the dashed curves represent contours of optimum junction depth, and the corresponding maximum responsivity versus lifetime for the two values of S is shown in Figure 3. For high value of S, the peak responsivity becomes saturated at high lifetime. It is also seen that the effect of the surface recombination velocity is more noticeable at high lifetimes than at low lifetimes.

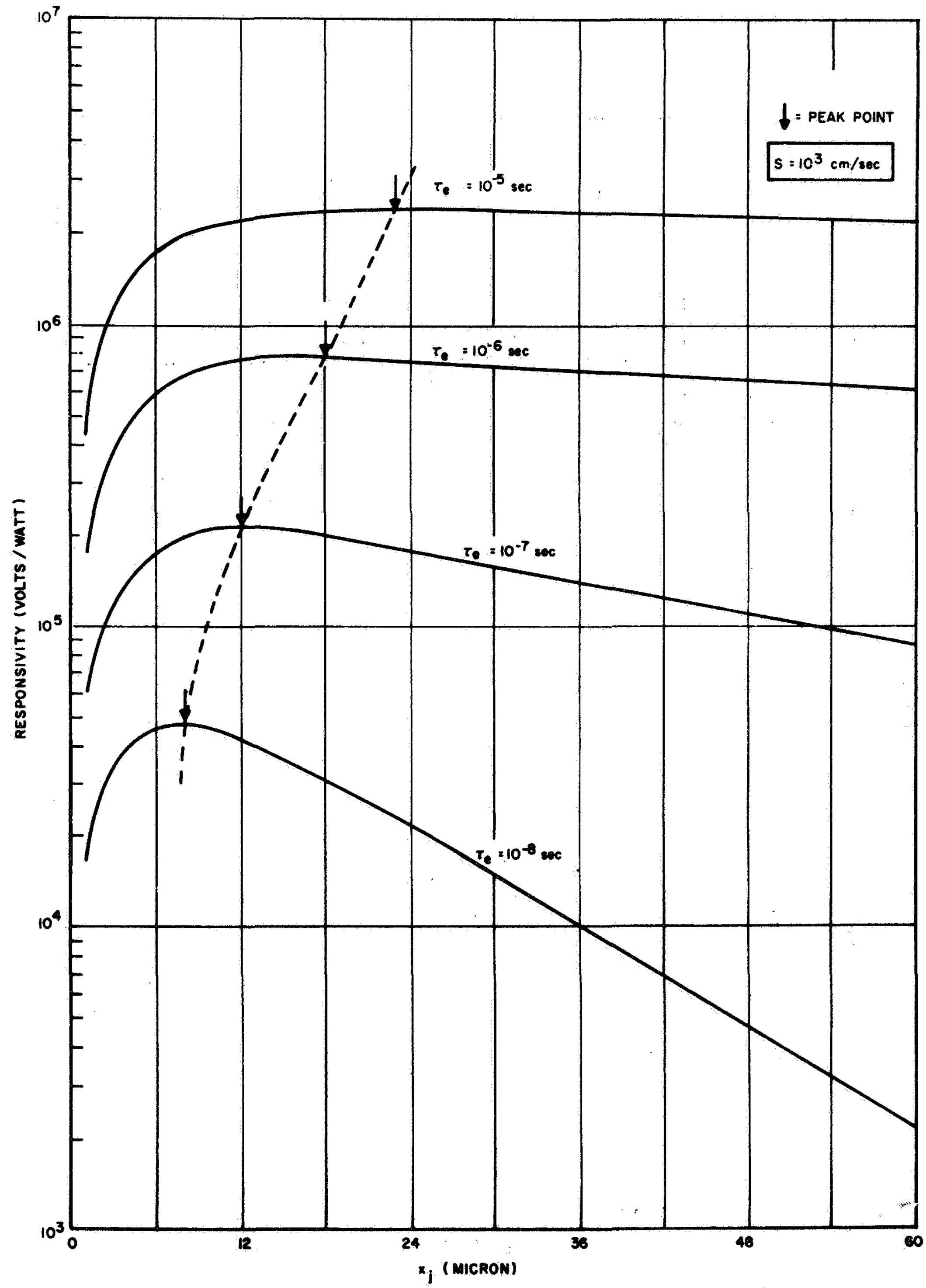


Figure 1. Responsivity versus Junction Depth for S = 10^3 cm/s

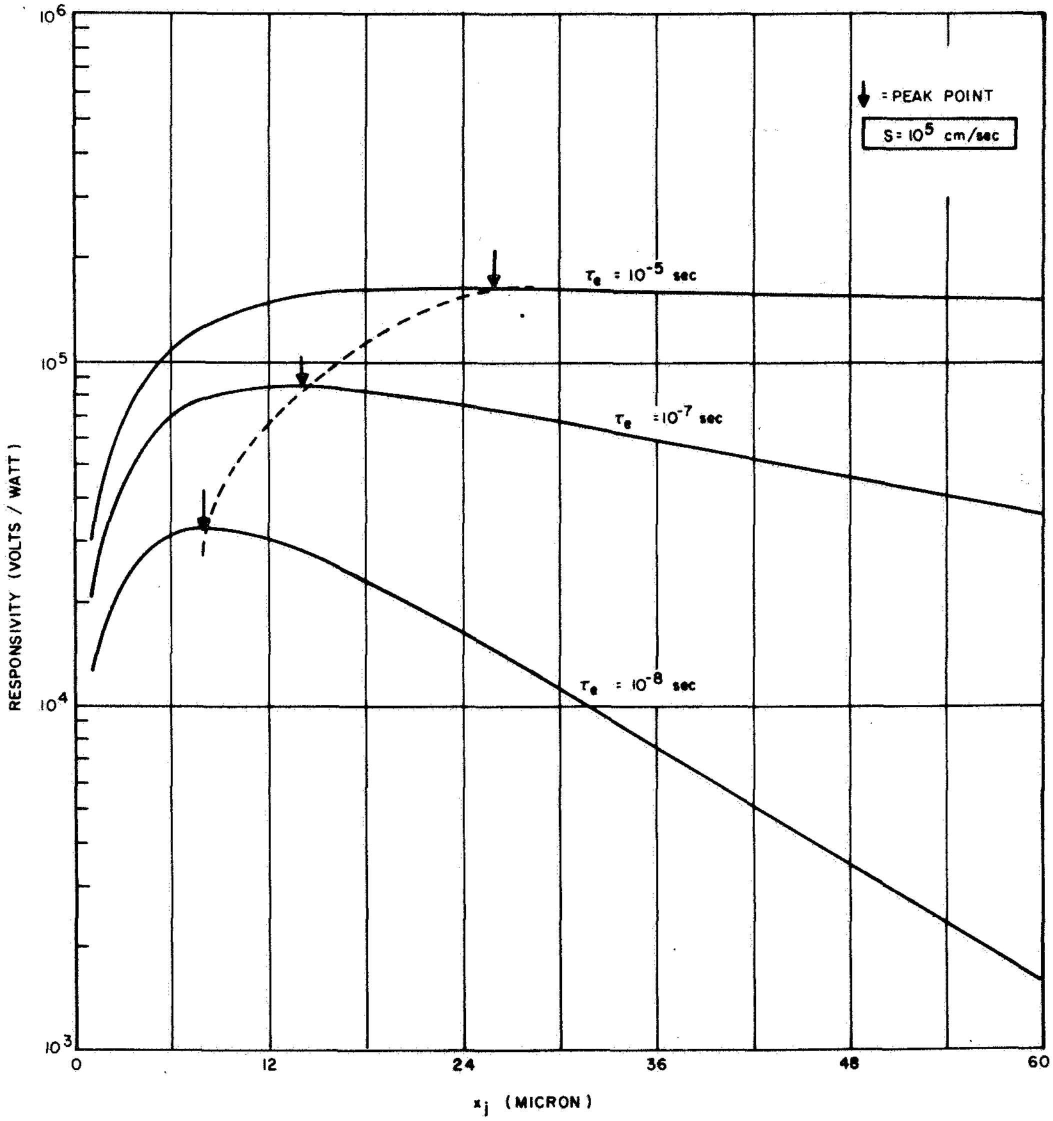


Figure 2. Responsivity versus Junction Depth for $S = 10^5$ cm/s

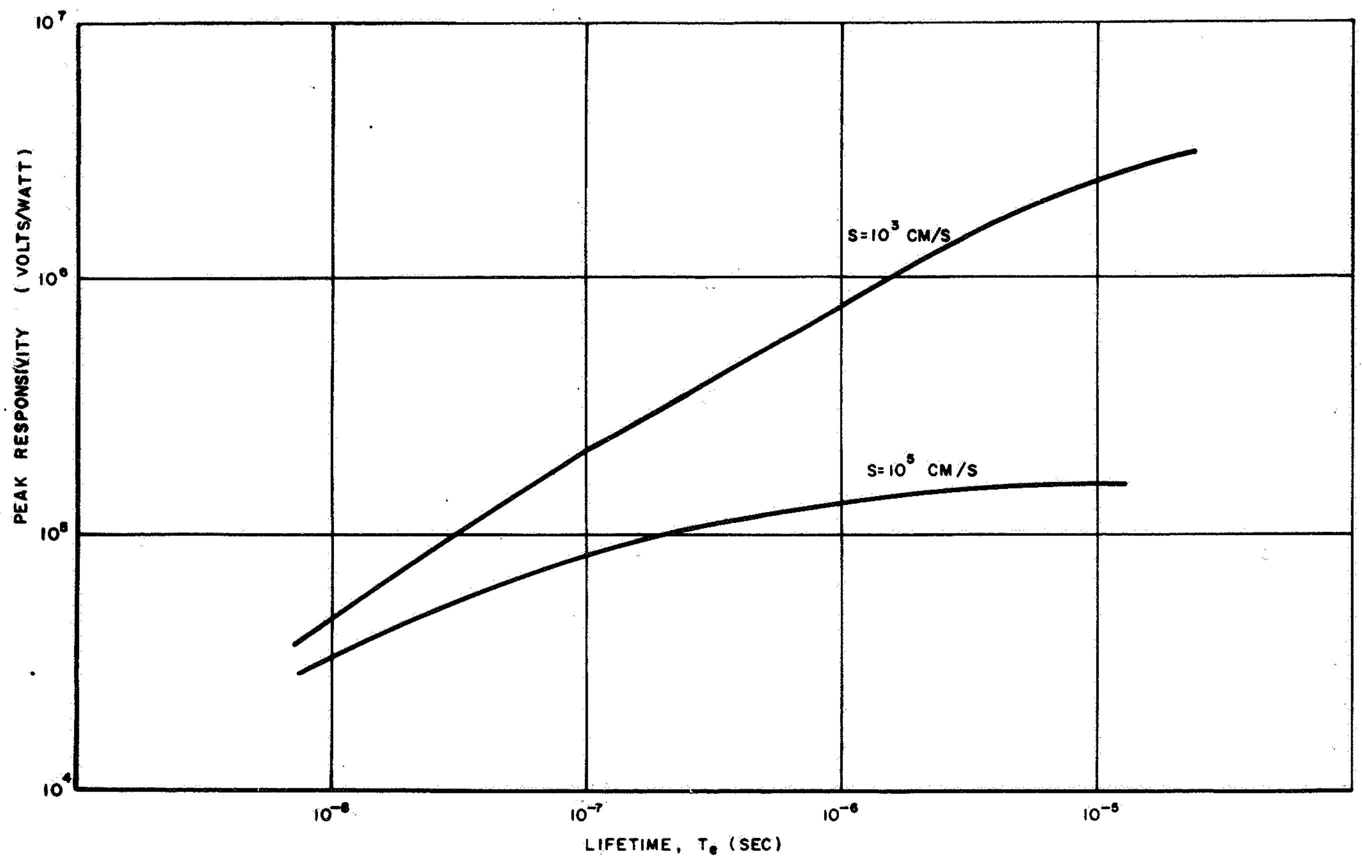


Figure 3. Peak Responsivity versus Lifetime

b. Noise of a Photovoltaic Diode

The noise of a photovoltaic diode is the thermal noise of the dynamic resistance of the junction at zero bias. The dynamic resistance, R of the diode, defined as the slope of voltage current curve at zero voltage derived in the Phase II report is given as:

$$R = \frac{L_e\left(SL_e \sinh x_0 + D_e \cosh x_0\right)}{q\beta A\left\{n_0 D_e\left(D_e \sinh x_0 + SL_e \cosh x_0\right) + \dfrac{p_0 D_h L_e\left(SL_e \sinh x_0 + D_e \cosh x_0\right)}{L_h \tanh \dfrac{(x_t - x_j)}{L_h}}\right\}} .$$

The thermal noise voltage for unit bandwidth is

$$V_n = \sqrt{4kTR}$$

The junction resistance, R, more or less is insensitive to the junction depth as expected, and therefore the noise voltage is nearly independent of the junction depth. For the optimum junction depths obtained from the responsivity analysis, the noise voltages were plotted as a function of lifetime as shown in Figure 4. The noise voltage increases with lifetime; it rises faster for the low value of S than for the high value of S. This is attributed to the fact that the diode impedance becomes larger as lifetime increases and surface recombination velocity decreases. This means the device impedance gets higher as the diode improves its characteristic. These effects have been observed in our experiment, as will be seen later in this report. The diodes having better device characteristic always give higher noise voltages than those of poor characteristic. Note that the responsivity rises faster than the noise voltage with the device improvements.

c. Detectivity D*

In the Phase II report, D* was also derived, and the result is:

$$D^*_\lambda = \frac{5.04\times 10^{18}\lambda\alpha T_e\left\{L_e(\alpha D_e + S) - \left[D_e \sinh x_0 + SL_e \cosh x_0 + \alpha L_e(SL_e \sinh x_0 + D_e \cosh x_0)\right]e^{-\alpha x_j}\right\}\left\{n_0 D_e(D_e \sinh x_0 + SL_e \cosh x_0) + \dfrac{p_0 D_h L_e(SL_e \sinh x_0 + D_e \cosh x_0)}{L_h \tanh \dfrac{(x_t - x_j)}{L_h}}\right\}^{\frac{1}{2}}}{2(\alpha^2 L_e^2 - 1)\left\{n_0(SL_e \cosh x_0 + D_e \sinh x_0) + \dfrac{p_0 L_e D_h(SL_e \sinh x_0 + D_e \cosh x_0)}{L_H D_e \tanh \dfrac{(x_t - x_j)}{L_h}}\right\}\left\{L_e(SL_e \sinh x_0 + D_e \cosh x_0)\right\}^{\frac{1}{2}}}$$

D* versus lifetime for the optimum junction depth is shown in Figure 5 for the two values of S. For high value of S, D* increases slowly and then is quickly saturated, whereas for low value of S, D* rises steadily up to the lifetime of 10 μsec and then appears to be saturated. The values of D* computed from the above equation and the assumed parameters are in reasonable agreement with available experimental data.

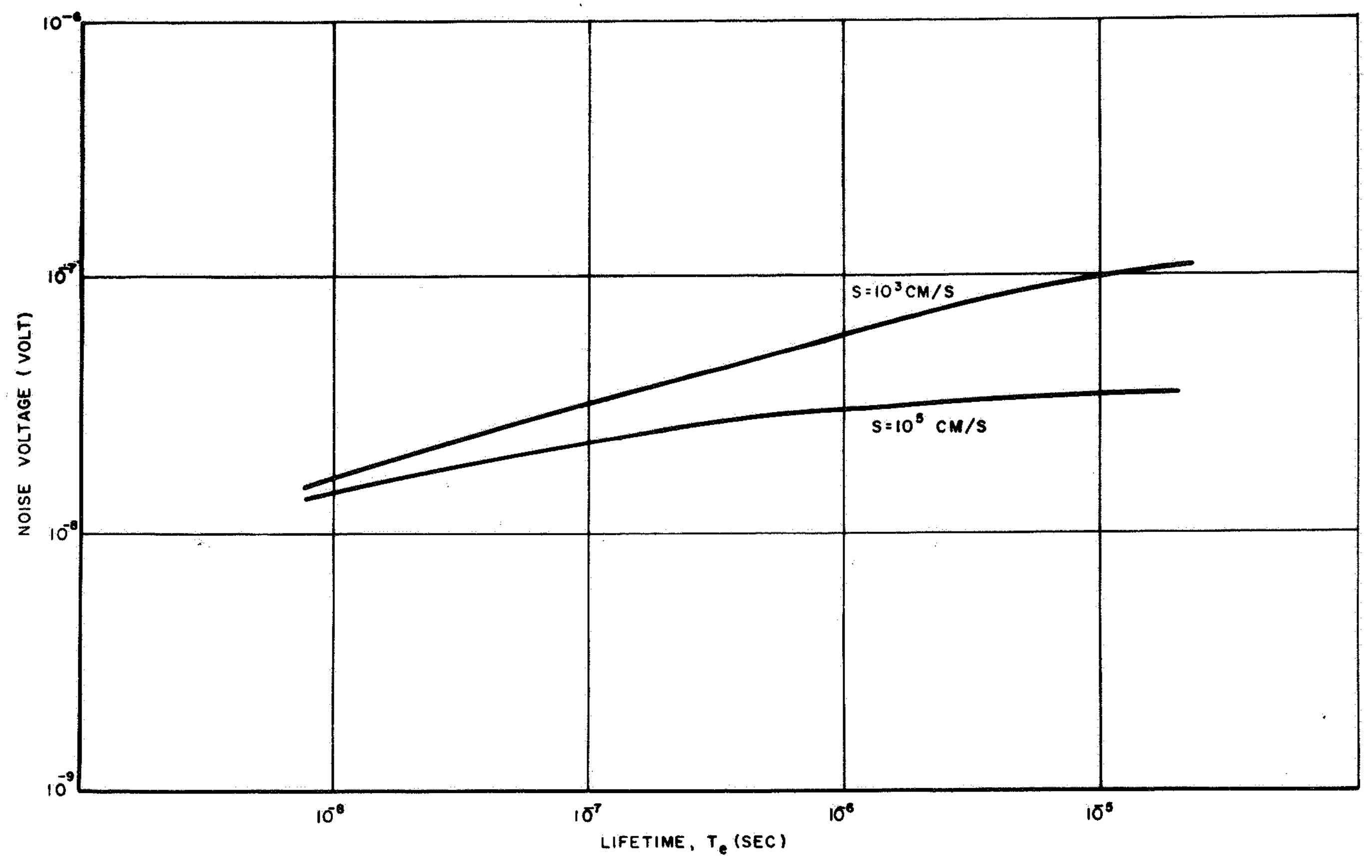


Figure 4. Noise Voltage versus Lifetime for the Optimum Junction Depth

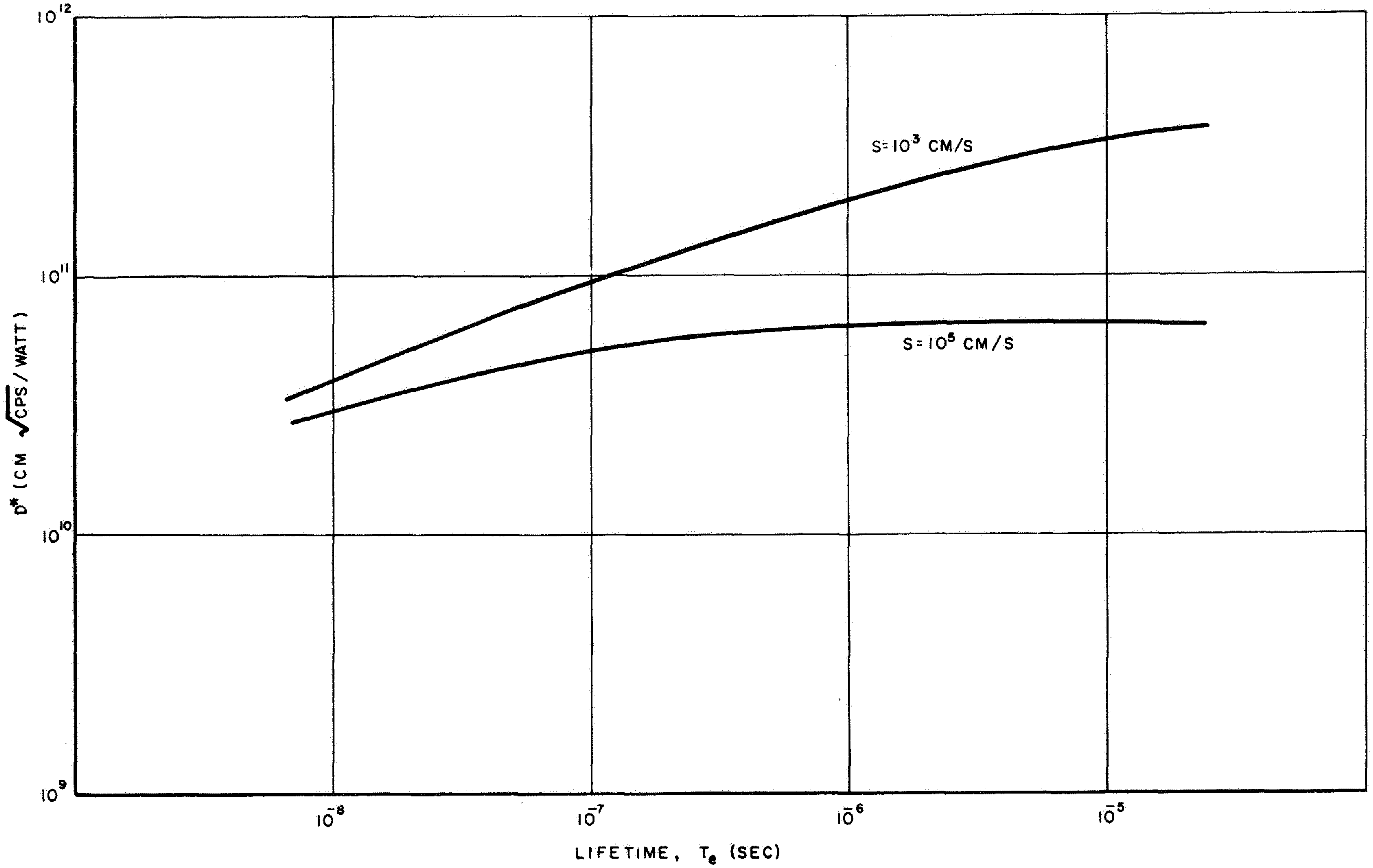


Figure 5. D* versus Lifetime for Optimum Junction Depth

d. Summary

Some of the results are summarized in Table III.

TABLE III. SUMMARY OF DETECTIVITY CALCULATION RESULTS

S(cm/s)	τ_e(sec)	Res. (ohm)	Noise V_n(volt)	D*(cm cps$^{\frac{1}{2}}$/watt)
10^3	10^{-5}	9.1×10^5	1.0×10^{-7}	3.3×10^{11}
	10^{-6}	3.1×10^5	5.8×10^{-8}	1.9×10^{11}
	10^{-7}	9.0×10^4	3.2×10^{-8}	9.4×10^{10}
	10^{-8}	2.4×10^4	1.6×10^{-8}	3.96×10^{10}
10^5	10^{-5}	1.1×10^5	3.4×10^{-8}	6.6×10^{10}
	10^{-6}	7.8×10^4	2.9×10^{-8}	6.3×10^{10}
	10^{-7}	4.6×10^4	2.3×10^{-8}	5.1×10^{10}
	10^{-8}	1.9×10^4	1.5×10^{-8}	3.0×10^{10}

From these theoretical results, some general conclusions for sensitive InAs photovoltaic detectors can be drawn:

1) For maximum responsivity or sensitivity, the lifetime should be as high as possible and the surface recombination velocity should be as small as possible. The lifetime is more critical than the surface recombination velocity to increase the sensitivity.

2) For high lifetime or diffusion length, the optimum junction depth is not too critical as long as the peak point is reached as shown in Figures 1 and 2. Our experimental results, as seen later, show that the sensitivities of the diodes diffused for 0.5 to 1.5 hours respectivity, are practically the same, indicating that the junction depths do not affect the device performance. This may indicate that the carrier lifetime in our devices is in the range of 1 - 10 μsec, which is not unreasonable to assume.

3) For low diffusion length, the optimum junction depth is very critical and the sensitivity decreases very rapidly with the junction depth. This effect has not been observed in our experiments, however.

4) The effects of the surface recombination velocity on the device performance are more noticeable at high lifetime than at low lifetime. It appears that the value of S of 10^3 cm/sec is likely to be encountered in our InAs devices.

5) The noise voltage of the photovoltaic diode increases as the diode improves its characteristic, due to the higher diode dynamic impedance. However, the sensitivity increases faster than the noise, and thus the detectivity D* is always higher for sensitive detectors. Our experimental results show this effect; the sensitive detectors always give higher noise voltage than poor detectors.

Note that the above analysis has been based on one wavelength and absorption coefficient; thus, the results should be changed for different wavelength and absorption coefficient. However, the wavelength used here, $3.3\ \mu$ is the typical peak response for the operating temperature of $200^{\circ}K$ for an InAs photovoltaic detector. Further analysis for different wavelength and temperature is needed to design optimum detectors for different applications.

It should be noted that p_o and n_o are inversely proportional to the sensitivity. However, in our experiment, reducing n_o by doping higher carrier concentration in the p-region gives less sensitivity than the lightly doped detectors. This may be due to the fact that higher doping concentration in the p-region tends to degrade the carrier lifetime, and as a result, the effect is to decrease the lifetime more than to increase the minority carrier density, n_o. This is why Cd-diffused InAs detectors are far more sensitivie than Zn-diffused diodes.

The following sections will discuss the development of InAs photovoltaic detectors, fabrication of InAs detector arrays, and the measurements of these devices. The theoretical results agree qualitatively with the results of the experiments.

B. DEVELOPMENT OF InAs P-N JUNCTION PHOTODETECTORS

1. Introduction

Most of the development in III-V compound semiconductors, as infrared photodetectors, has been devoted to InSb, and considerable progress in the device technology has been made. The studies of InAs have not been as extensive as InSb. This may be partly due to the fact that the purification of InAs is more difficult than InSb. Thus, InAs photodetectors have received relatively less attention, and the basic device technology has not yet been fully exploited; as a result, information for InAs device processing is not readily available in the literature.

Unlike InSb, reaction of the elements to form the compound is not a simple matter. Because of the high volatility of arsenic, it is quite difficult to fabricate InAs devices at high temperature, as the arsenic is easily lost from the surface. The lack of arsenic in the InAs crystal will result in a non-stoichiometry which will destroy the crystal properties. Thus, the device processing is extremely critical and extra attention must be given to each processing step.

The InAs photovoltaic detector whose characteristics were calculated in the previous section has been successfully fabricated. This section describes the process used in developing the device fabrication techniques for a high sensitivity InAs photodetector. Part of the process has been used in fabrication of InAs array sensors which will be discussed later in this report.

2. Wafer Preparation

Single-crystal tin-doped n-type InAs ingot materials with carrier concentrations in the range of 2.5×10^{16} to 3.0×10^{16} carriers/cm^3 and with mobilities in excess of 25,000 cm^2/volt-sec. have been purchased from Monsanto in St. Louis, Missouri. The crystals were grown by the Czochralski method with 111 orientation. The following general criteria were used in selecting these materials:

1) Minimum dislocation density
2) Maximum carrier mobility
3) Uniform distribution of impurity density.

Wafers were prepared by slicing, with a wire saw, to a thickness of about 20 mils and to an area of one cm diameter. Both sides of the wafers were lapped to flat and parallel surfaces. Then the B-face (arsenic side) was polished mechanically to a mirror-like surface. After mechanical polishing, the surfaces were further polished with 5% bromine and 95% methanol to remove any scratches resulting from the mechanical polish.

Note that it is quite difficult to polish the A-faces (indium side). In fact, the chemical polish resulted in etchpits on the surface. However, the polished B-faces appeared to be scratch-free and optically flat.

The polished wafers were removed from the holders and soaked and boiled in trichloroethylene to remove the black wax, and then were degreased in fresh trichloroethylene vapor.

The cleaned wafers were stored and kept in isopropyl alcohol until ready for the next process. Prior to loading into furnace for pre-oxidation, the wafers were etched with HF, washed thoroughly in separate baths of distilled water, and were allowed to dry in air on a clean filter paper.

3. Deposition of Diffusion Mask

In order to fabricate high-density multi-element detector arrays of InAs, selective masking against diffusion is required to construct multiple structures. Since InAs, unlike silicon, does not have a native diffusion mask, it is necessary to deposit a foreign diffusion mask on InAs substrates. The deposition of such a mask with good effectiveness of masking against high temperature diffusion is not simple; thus, a special techinque is required.

A technique for depositing SiO_2 on III-V compound semiconductors and metals has been developed at the Electronics Laboratory of the General Electric Company.[2] The deposition involves the glow discharge decomposition of an organic silicate in an oxygen plasma atmosphere at room temperature.

[2] See Phase II Technical Report.

Since it is processed at room temperature, a possible surface deterioration of the InAs from loss of the voltatile arsenic is not encountered during such deposition.

It has been found, however, that in order to adhere the SiO_2 well to the InAs surface, it is required to pre-oxidize the surface. The pre-oxidation was carried out in an oxygen atmosphere at 500°C for 10 min. This pre-oxidation gave a native indium oxide on the InAs surface on which the deposition of SiO_2 was excellent.

It has also been found that the pre-oxidation of InAs prior to the SiO_2 deposition is very critical. If the indium oxide is too thick, it is decomposed by the SiO_2 at diffusion temperature; on the other hand, if the indium oxide is too thin, the SiO_2 does not adhere well to the surface. The proper thickness of the preoxide was determined and controlled from wafer to wafer by observing the surface color.

If the silicon oxides are not properly deposited on the InAs wafers, it is extremely difficult to fabricate multi-element InAs detector arrays with a high degree of uniformity between individual elements. It has been found that the fast deposited SiO_2 layers cracked during the diffusion and did not mask the selected areas. The thickness of the deposited silicon oxide layers that gave a satisfactory result was measured to be approximately equal to 2500Å. The properly deposited oxides always gave sharp resolution when the windows for the detector element were etched by means of the photoresist process, which is to be discussed next.

4. Photoresist Process

The areas to be diffused were delineated by means of a photoresist etching technique; a combination of photographic and chemical etching techniques. Because of the deposited SiO_2, the standard technique for silicon can not be used, and thus an applicable process should be determined to obtain an optimum result. The following processes have been found to give satisfactory results:

1) Photoresist coating: The silicon oxide-deposited surface was coated with KMER at about 400 rpm for 10 sec, and then allowed to dry in air for 30 min.

2) Prebake: The resist-coated sample was dried at 80°C for 30 min. The sample was then ready for exposure.

3) Exposure: Using an appropriate mask, the sample was exposed in an exposure machine for 4 sec. The unexposed areas were developed and the resist removed from them.

4) Postbake: The exposed resist on the sample was baked at about 150°C for 24 hours to give a good chemical resistance of photoresist. The sample was then ready for chemical etching for the silicon oxide.

5) Etching: The unmasked SiO_2 was then etched in a buffered ammonium bi-flouride solution until all the unprotected

SiO_2 was etched away. The etching time usually ran for about 1.5 min.

6) Resist removal: After etching the SiO_2, the masked photoresist was removed by A-20 stripper and the wafer was rinsed in warm running distilled water. The finished sample was then degreased in trichloroethylene vapor and stored in propanol till next process. Typical sharp resolution etched windows of the oxide diffusion mask on an InAs wafer are shown in Figure 6. The wafer was then ready for diffusion.

5. Diffusion Process

For the fabrication of p-n junction photovoltaic sensors, the diffusion technique is very important, not only because it controls the uniformity of detector characteristics but also the sensitivity of the detectors. Unlike Si and Ge, the diffusion of impurities into III-V compounds is much more complicated because the compounds tend to dissociate and lose the more volatile element (Group V) at diffusion temperatures and both elements (i.e. In and As) have a greater tendency to react chemically with the diffusion impurities.

All diffusion processes have been carried out in sealed silica ampoules evacuated to approximately 10^{-5} to 10^{-6} mm Hg. Prior to use, the inside of the ampoules was cleaned by soaking in a White Etch 41 for 30 min. This cleaning etched the surface of the tube slightly to give a clean finish. The tube was then thoroughly rinsed in several changes of distilled water, and evacuated to about 10^{-7} torr. Then the ampoule was baked at about 900°C by flaming the outside of the tube. The tube appeared to be very clean and was kept in vacuum until ready for diffusion.

Sample boats used for the insertion of the wafers, doping charge, and background source into the ampoule were made from ultra-high purity graphite as shown in Figure 7. The boat was designed to obtain symmetry along the ampoule tube for the wafers. The InAs wafers were loaded at the center of the boat, a background source (InAs powder) was loaded in the next two holes, and a dopant (In-Cd alloy) was placed in the last two holes of the boat. Since the boat was in direct contact with the sample, the boat was cleaned very carefully by soaking in a solution of 1:3 volumes of HNO_3 and HCl for two hours and then rinsing in distilled water. Finally, the boat was baked out in vacuum in order to remove any high vapor pressure materials remaining in the graphite which might contaminate the wafers during diffusion. Using this boat we have obtained uniform and reproducible p-n junction devices of InAs.

During the diffusion, the partial pressure of the more volatile constituent, arsenic, was controlled by providing extra arsenic in the diffusion ampoule as a background source. When there was no background source in the ampoule during the diffusion, the surface of the sample was severely pitted and very nonuniform. For satisfactory results, we have found that the use of InAs powder, as a background source, provides excellent surface conditions and a cleaner wafer surface than does pure arsenic. The powder was made from n-type polycrystal InAs ingot whose carrier concentration was about the same as that of the sample wafers.

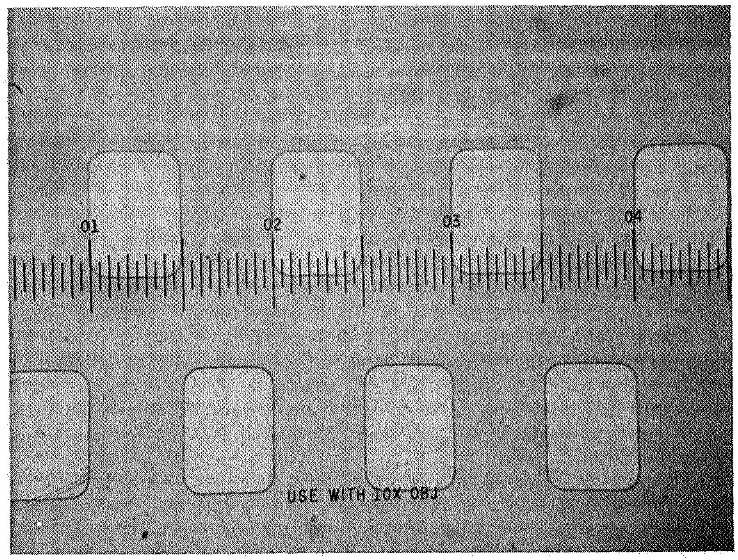


Figure 6. Deposited SiO_2 Diffusion Mask on InAs Substrate

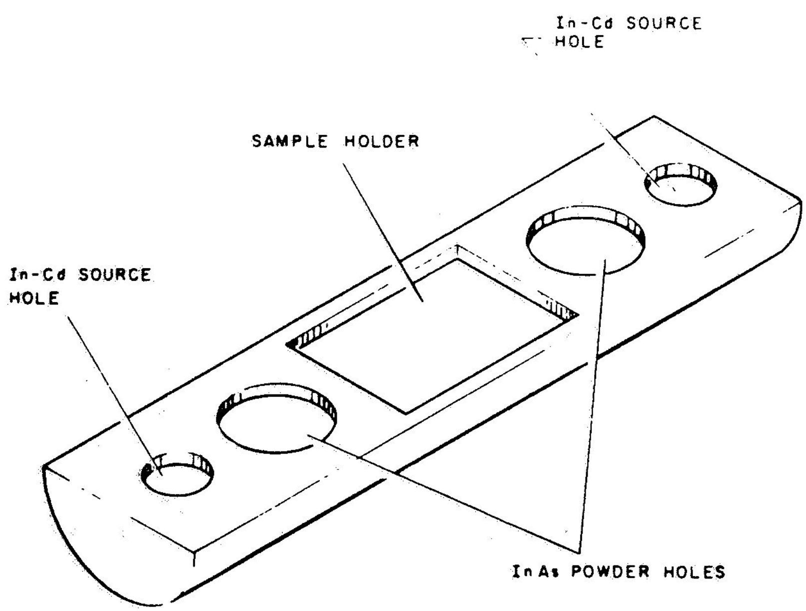


Figure 7. Graphite Diffusion Boat

The diffusants for acceptor impurity in III-V compound semiconductors, in general, have been Zn and Cd. Since these materials have a very high vapor pressure, it is usual to alloy them with a low vapor pressure material such as In or Ga. We have used an In-Cd alloy source for InAs as an impurity source for diffusion. The purpose of the alloy is to control the Cd vapor pressure, which in turn determines the surface concentration during diffusion. The doping levels in the diffused p-region can be thus controlled by varying the Cd content in the In-Cd alloy source.

The effect of Cd contents in the alloy on the device characteristics can be demonstrated in the following figures. Figure 8 shows a typical V-I characteristic of the diode diffused with a straight Cd source at 750°C for 40 min. Figure 9 shows a V-I characteristic of the diode that was diffused with 50% of Cd content in an In-Cd alloy source for one hour at 750°. A typical V-I characteristic of the diode fabricated by a two-step diffusion is shown in Figure 10. Two-step diffusion consisted of pre-diffusion and drive-in-diffusion; the pre-diffusion was carried out with a straight Cd source at 700°C for 15 min, and the drive-in-diffusion was done at 750°C for an hour without any impurity source. These diodes were fabricated without using any diffusion mask and by etching mesa structure after diffusion.

These diodes exhibit some degree of tunneling, indicating that the diffused acceptor impurity is "so" high and the junction is practically degenerated. The diode diffused with "a" straight Cd shows more abnormal characteristic than those of other two diodes. The diode of two-step diffusion exhibits a closer diode characteristic which appears more or less like that of a backward diode. This means that the acceptor impurity is still high.

The above results clearly indicate that a high Cd content source used in diffusion causes a poor junction characteristic. In some cases, the InAs surface was damaged showing some etch-pits when a high Cd content source was used in diffusion. The two-step diffusion appears to give a lower impurity doping, but because of the additional processes involved it has been difficult to control uniform and reproducible devices. Instead, all efforts were directed to control the Cd concentration in the In-Cd alloy source for one-step diffusion, It will be seen later that a considerable decrease in the Cd content of the alloy dopant source leads to an excellent junction characteristic and a sensitive photovoltaic detector diode.

Many diffusion runs have been performed in order to determine an optimum diffusion condition. An hour diffusion at 740°C with a 3% Cd-97% In alloy source appears to produce optimum device characteristics. The In-Cd alloy sources were formed in a hydrogen alloy station by mixing pure Cd and pure In in proper portions at about 400°C. The low Cd concentration in the alloy source has been proved to give excellent results, which will be discussed later.

Junction Observation:

The diffusion process and the optimum design of any junction devices both depend on the junction depth and flatness. To measure these, both chemical delineation and staining techniques have been commonly used. While junction

300° K 77°/C

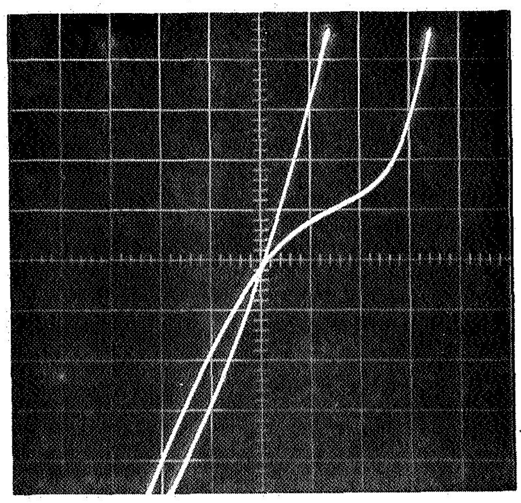


Figure 8. V-I Characteristic of Diode Diffused With Straight Cd.
(Scale: V=20 ma/div. H=0.1 volt/div.)

300° K 77° K

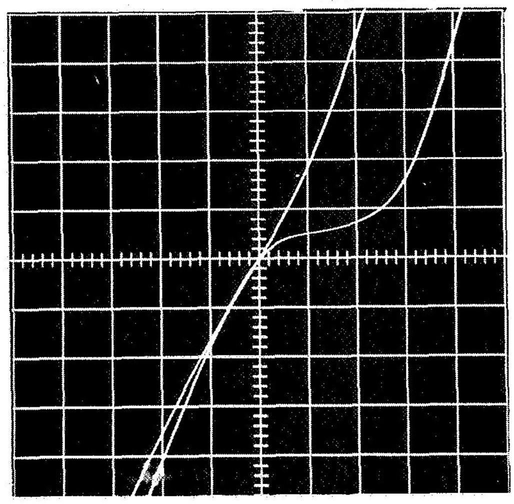


Figure 9. V-I Characteristic of Diode Diffused With 50% Cd.
(Scale: V=10 ma/div. H=0.1 volt. div.)

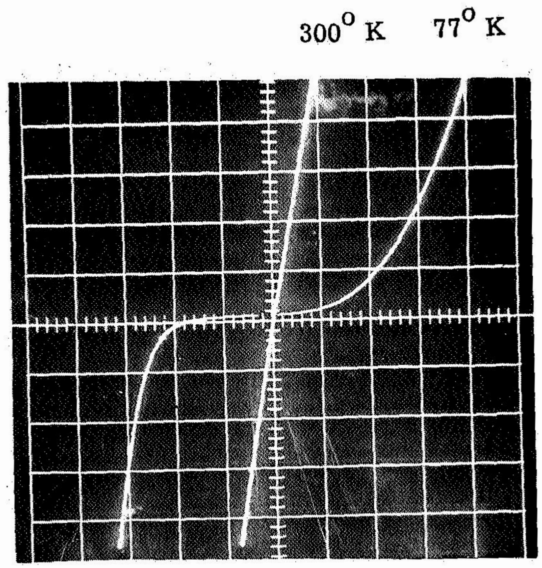


Figure 10. V-I Characteristic of Diode of Two-Step Diffusion. (Scale: V=20 ma/div. H=0.1 volt/div.)

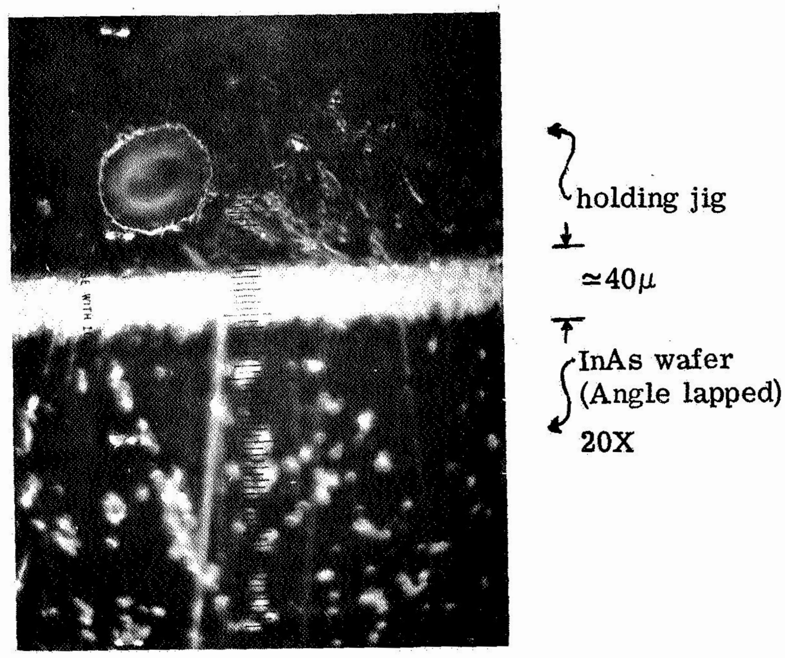


Figure 11. Typical Photograph of Stained P-region

delineation methods for the more common semiconductors are readily available, this is not the case for InAs. The normal staining technique that is used for Si, Ge, and GaAs is more difficult to use with InAs because the intrinsic carrier concentration at room temperature is so high.

However, heavily doped p-regions have been observed by staining. After diffusion with a straight Cd, the diffused sample was lapped and polished at some convenient low angle to the original surface to obtain the necessary magnification. A droplet of gold chloride solution (0.66 grams of $HAuCl_4 3H_2O$ in a liter of water) was then placed on the polished cross-sectioned surface under a strong light for one minute. After rinsing with water, a droplet of a solution containing 5 parts of water, 2 parts of HF, and 2 parts of H_2O_2 was placed on the surface for one minute. The etch stains the heavily doped p-region as shown in Figure 11.

It is interesting to note that unpolished samples gave better junction delineation than the polished ones though both unpolished and polished samples were diffused at the same time. This indicates that the unpolished samples have been diffused with higher carrier concentration than the polished samples when they are diffused at the same time.

For the samples diffused with low Cd concentrations, it was difficult to observe clear junction definitions at room temperature. An attempt was made to delineate the lightly doped junction by an anodic oxidation, but no successful result was obtained. Since a lightly doped junction is required for a sensitive InAs photodetector, it is clear that no common junction stain that is used at room temperature can be employed to observe the true junction of the InAs diode.

6. Ohmic Contact

Ohmic contacts to both p-type and n-type InAs semiconductors were obtained by means of vacuum deposition and alloying techniques. For p-type diffused regions, 5% Cd with 95% Au and for n-type materials, 5% Sn with 95% Au were used, respectively. Addition of a small amount of In to the alloys appears to give a good result.

In order to insure that the contacts were ohmic, the following experiments were performed. Two dot contacts were made to an n-type InAs sample by evaporating Au-Sn through a metal evaporation mask. The contacts were subsequently alloyed to the InAs in a hydrogen alloy station. Likewise, two ohmic contacts to a p-type diffused region were made by alloying evaporated Au-Cd dots. V-I characteristics of the ohmic contacts were measured by probe contact to the alloyed dots, and observed to be linear. Nonlinear characteristics were observed when the probe made a point contact to the InAs surface.

The evaporated ohmic contact on the back side of the substrate not only serves as an ohmic contact, but also provides good conduction of heat to the heat sink header. The alloys for ohmic contacts were made at about 420°C. Since this temperature is far below the diffusion temperature, it does not affect the diffused junctions which were made at a temperature of 740°C. These ohmic contacts gave satisfactory results, and no particular problems for ohmic contact were encountered.

7. Surface Treatments

The device characteristics were observed to be a strong function of the surface treatments after diffusion. The indium oxide on the surface, which had been used in order to deposit the SiO_2 diffusion mask, acted as a surface conducting channel as will be seen later, and consequently increased the diode reverse saturation current. To remove such oxide after diffusion, it was necessary to etch the surface and to give special surface treatments. All single devices studied here were planar structures, and the active area was chosen to be 0.05×0.05 inches. This large area was used to develop a technique for a planar process.

The effect of indium oxide and SiO_2 on the device characteristics is demonstrated in the following figures. Figure 12 is the diode V-I curve of Sample # 28 without removing the SiO_2 diffusion mask, and as seen the diode exhibits large leakage current. When the oxide was removed, the device characteristic was somewhat improved as shown in Figure 13. If the same device characteristic was cleaned with HF for 10 min, the diode showed further improvement as demonstrated in Figure 14. These results clearly indicate that in order to improve the diode characteristic, the diffusion mask must be removed after diffusion and the surface must be etched and cleaned.

After removing the SiO_2 with HF, the diode that had been etched in a strong HNO_3:HF:H_2O solution, exhibited a distinctive improvement of its diode characteristic. A problem in etching the surface with a strong etchant was a tendency to destroy the surface uniformity and flatness. Thus, a weaker etchant was required and a solution of 5:3:3 of HNO_3:HF:H_2O was found to give good results. An optimum etching time was found to be about 10 sec.

Further improvement on the device characteristic was obtained by a special chemical treatment. The strong oxidizing agent in the etching solution used usually attacks the arsenide more than the indium on the InAs surface. As a result it appears that the etching leaves an indium-rich non-stoichiometric surface on the InAs, which in turn readily oxidizes. As discussed before, the indium oxide degrades the device characteristic.

In order to treat the etched surface, the following solution of

1.5 gm Ethylenediaminetetraacetic acid (EDTA)

0.3 gm Potassium hydroxide (KOH)

0.3 gm Tartaric acid

100 ml Distilled water

was used. After the chemical etching, the devices were soaked in the above solution for prolonged time. A typical V-I characteristic of the diode treated with the EDTA over night is shown in Figure 15. As seen, the diode has been improved considerably over the diode with SiO_2 (Figure 12). These diodes were diffused with 5% Cd alloy source for an hour at 740°C.

No noticeable surface change was observed after the treatment with the EDTA. The exact mechanism, of reaction of this solution with the InAs

77°K

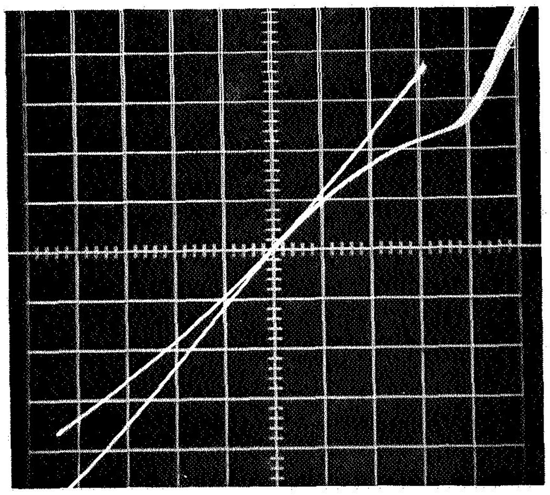


Figure 12. V-I Characteristic of Sample #28
with oxide
(Scale: V=10ma/div. H=0.1 volt/div.)

77°K

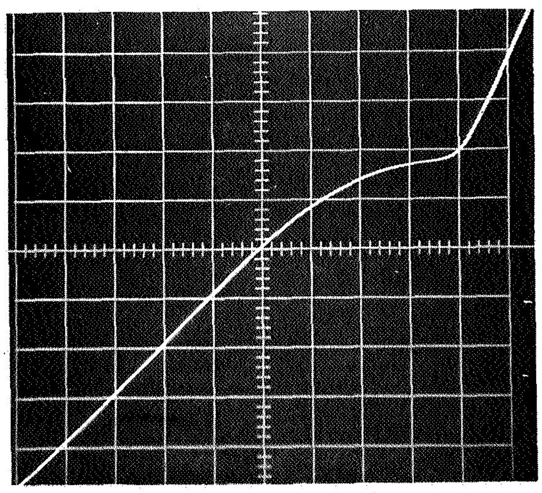


Figure 13. V-I Characteristic of Sample #28
with oxide removed
(Scale: V=10ma/div. H=0.1 volt/div.)

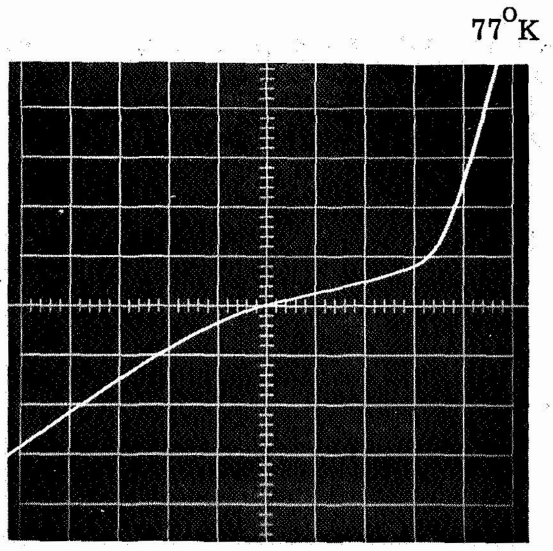


Figure 14. V-I Characteristic of Sample #28
Etched in HF for 10 min.
(Scale: V=10ma/div. H=0.1 volt/div.)

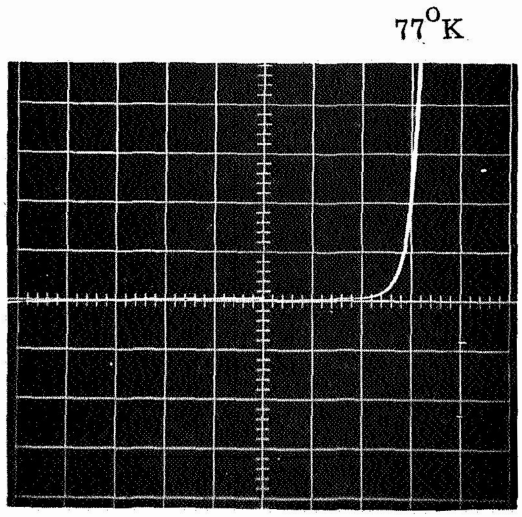


Figure 15. V-I Characteristic of Sample #30A
Soaked in EDTA over night
(Scale: V=1 ma/div. H=0.1 volt/div.)

surface is not yet known, but the complexing agents, such as EDTA, have been used to dissolve metallic ions on the surface of semiconductors. This indicates that the above solution of EDTA may preferentially attack or dissolve the indium-rich surface, resulting in a more nearly stoichiometric InAs surface.

The effect of the indium oxide on the device characteristic was demonstrated by the following experiment. A device that had been processed through all the above steps showing a good V-I curve, was anodized over the whole surface. The characteristic after the anodic oxidation is shown in Figure 16, and the curve for which the oxide has been subsequently removed with HCl solution is also shown in the same figure. It is clear that the indium oxide, indeed, increases the surface leakage.

The surface passivation of InAs planar diode was accomplished by vacuum deposition of arsenic trisulfide (AS_2S_3). Figure 17 shows the V-I characteristic of a diode passivated with As_2S_3. To measure the breakdown voltage of a vacuum-deposited arsenic trisulfide thin-film insulator, an As_2S_3 film was sandwiched between two thin-film metal electrodes. The breakdown voltage across the films was measured to be 60 volts. This indicates that the aresenic trisulfide film can be used as an insulator on the device surface so as to fanout the leads by etched thin-film conductors for array fabrication. It was found, however, that the arsenic trisulfide melts near 300°C. Therefore, after deposition of As_2S_3, the device processing temperature must be less than 300°C.

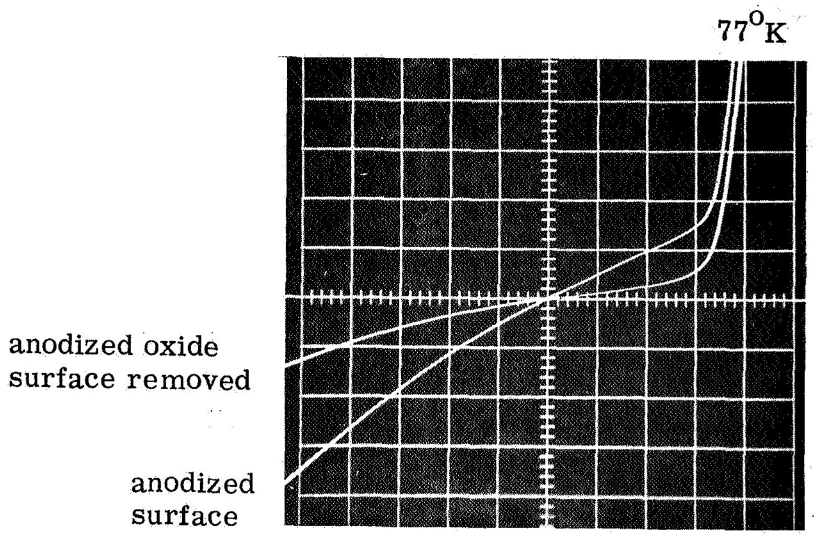


Figure 16. Typical V-I Characteristics of Sample #30A after anodized surface and removed with HCl
(Scale: V=5ma/div. H=0.1 volt/div.)

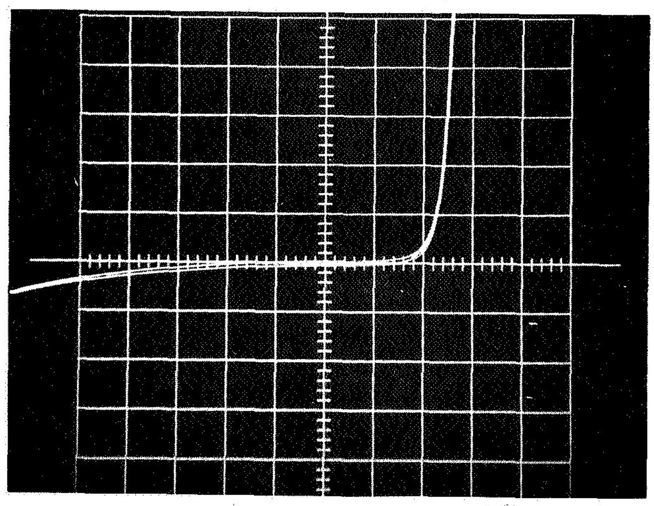


Figure 17. V-I Characteristics of Sample #34-A Passivated with As_2S_3
(Scale: V=10 μa/div. H=0.1 volt/div.)

8. Summary

Some of the results developed in this section for large junction area, discrete, planar InAs infrared photodetectors are summarized in Table IV. The corresponding diffusion conditions are also shown in Table V.

TABLE IV.

SUMMARY OF DISCRETE DEVICE DETECTORS

Sample No.	Temperature (T^oK)	Signal Voltage (volts)	Dark Noise Voltage (volts)	D* cm. $cps^{\frac{1}{2}}$/watt
30A	77^oK	6.2×10^{-5}	5.0×10^{-8}	4.8×10^{8}
	153^oK	1.2×10^{-4}	2.0×10^{-8}	2.4×10^{9}
31	77^oK	1.4×10^{-5}	2.0×10^{-8}	2.6×10^{8}
	153^oK	2.2×10^{-5}	2.5×10^{-8}	3.4×10^{8}
32	77^oK	6.6×10^{-6}	1.4×10^{-8}	1.8×10^{8}
	153^oK	1.9×10^{-5}	1.8×10^{-8}	4.2×10^{8}
34A	77^oK	1.2×10^{-3}	7.0×10^{-7}	6.7×10^{8}
	153^oK	4.3×10^{-4}	7.0×10^{-7}	2.4×10^{8}

TABLE V.

SUMMARY OF DIFFUSION CONDITIONS

Sample No.	Diffusion Source	Diffusion Temp. (^oC)	Diffusion Time
30A	6% Cd	740	1.0 hour
31	6% Cd	740	1.5
32	10% Cd	740	0.5
*34A	3% Cd	740	1.0

(*) The surface was passivated with arsenic trisulfide (As_2S_3).

The D* measurements were made with a blackbody temperature of 500^oK and chopping frequency of 625 cps. Detailed optical measurements are discussed later in this report.

The diffusion condition for Sample #34A appears to be an optimum condition, and its signal voltage is two orders of magnitude greater than those of other devices diffused under different conditions. However, the noise voltage is also increased as shown in Table V. Note that, as the device is improved, the signal is increased as well as the device noise. The higher noise is attributed to the higher diode impedance, which is inversely proportional to the reverse saturation current. It is interesting to note that the devices fabricated with higher Cd concentration in the diffusion source exhibit signal voltages at $153^{o}K$ that are consistently higher than those at $77^{o}K$. A further effort is needed to study this effect.

Some of the processing techniques developed in this section will be utilized in the development of array fabrication in the following section. As will be seen, however, due to the complicated array fabrication, new techniques are required to complete array process. These are discussed in the next section.

C. FABRICATION OF InAs PHOTOVOLTAIC DIODE ARRAYS

1. Introduction

Unlike the descrete device fabrication, the array fabrication processes are more complex and difficult since the array sensors consist of a mosaic of individual sensitive elements. The requirements imposed upon these mosaics of multi-element diode arrays are high-density patterns of very small elements of extreme dimensional accuracy, coupled with a high degree of uniformity of the electrical and optical characteristics of the individual diode elements.

The array dimensions are fifty 5×7 mil diode elements, spaced 10 mils apart center-to-center, in a 2×25 staggered line array, part of which is shown in Figure 6. The array fabrication process has been started with the optimum processing conditions obtained from the discrete device fabrication discussed in the previous section, but it requires some additional techniques to achieve uniform and sensitive detector diodes in the array.

The array fabrication process is the same as before up to the diffusion process discussed in the previous section for the discrete device fabrication, and the optimum conditions have been utilized. All diffusions were well under control, with reproducible device characteristics being obtained. Therefore, it has been possible to diffuse several wafers during each diffusion run to save time and materials.

However, the post-diffusion surface preparation and the final assembly steps have been found to be extremely critical in the array fabrication. The following sections will describe the processes developed for both planar and delineated arrays. Along with these processes, the problems associated with the array fabrication will also be pointed out.

2. Planar Array Process

Since all the processes up to the diffusion are the same as before, the planar processing steps after the diffusion are described as follows:

a. Post-diffusion Surface Preparation

After diffusion, the SiO_2 was removed by etching the surface, except along the periphery of the wafer. This remaining oxide was used as a supporting insulator for wire bonding. A critical problem in etching the surface was a tendency of the etching process to destroy the surface uniformity and flatness. Therefore, care must be exercised not to remove the diffused windows completely but to leave some visible pattern of the diffused p-regions, to make subsequent photographic processes possible.

b. Second Deposition of SiO_2

A second deposition of the silicon oxide was required to form a small ohmic contact to the diffused p-regions. Many attempts to place small ohmic contacts at the proper area of the diffused p-regions by means of a reverse strip technique remain unsuccessful to date. The deposition process was the same as before, and thus the surface must be etched and cleaned again after use.

c. Ohmic Contact

At the center of the diffused regions, 3×5 mil windows were opened and then the alloyed ohmic contacts were made as described before. This contact area was used to develop techniques for achieving good ohmic contact and if this technique is feasible, a new mask can be used to locate the contacts at one side of the diffused windows, thus maximizing the active areas for the optical signal.

d. Final Surface Etching

The indium oxide introduced during the second deposition of SiO_2 must be removed by etching the surface again. However, at this point, the surface etching must be accomplished carefully so that the metallized ohmic contacts will not be destroyed. A mild etching solution of 1:1:1 of HNO_3:HF:H_2O was used. After etching the surface, the array wafer was soaked in the EDTA for two hours and then rinsed with distilled water. Note that the EDTA solution did not attack the alloyed ohmic contacts. Figure 18 is a typical array, showing the diffused areas with the ohmic contacts after final surface etching.

e. Surface Passivation

Surface passivation of InAs is not only important to protect the surface, but also required to fan out the leads for array fabrication. To connect from the diffused diode elements in the array to the external circuits, it was necessary to use an insulator material for evaporated lead connection, as shown in Figure 19. It has been shown that the vacuum deposited arsenic

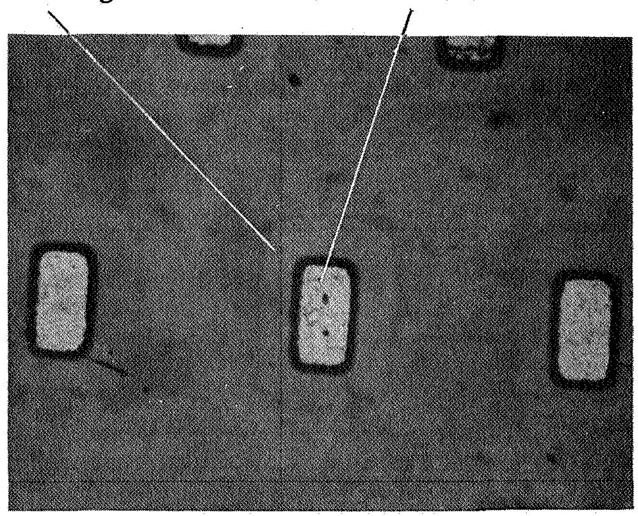


Figure 18. Typical Ohmic Contacts to the Diffused Areas

trisulfide (As_2S_3) thin film is an excellent surface passivation on InAs surface. However, the following problems in using this insulator with InAs have been found: (1) The film did not adhere well to the InAs surface, such that subsequent photographic processing was difficult. It was found, however, that the adherence can be improved by heating the InAs substrate during the deposition. The substrate temperature of 150°C appears to give good results, (b) The film was quite sensitive to certain chemicals used in the photoresist process - for example, the coated photoresist on the film could not be baked; it was removed by degreasing with trichloroethylene after the process; and (3) Since the film melts near 300°C, the deposited As_2S_3 on InAs substrates can not be heated more than 300°C for subsequent processing. For example, thermal compression wire bonding can not be used, because the required temperature is much higher than 300°C. An attempt was also made to use the photoresist as an insulating passivation material on the InAs surface.

f. Fan-out Leads

After opening the ohmic contact areas through the As_2S_3 insulator layer, gold metallization of the whole surface was made. Then the lead patterns were made, using Shipley's Az photoresist. It appeared, however, that the gold adherence to the arsenic trisulfide film was not good, but the use of aluminum for the fan-out leads appeared to be excellent. Its adherence to the film and photoresist was better than that of gold. A completed typical fan-out array is shown in Figure 20.

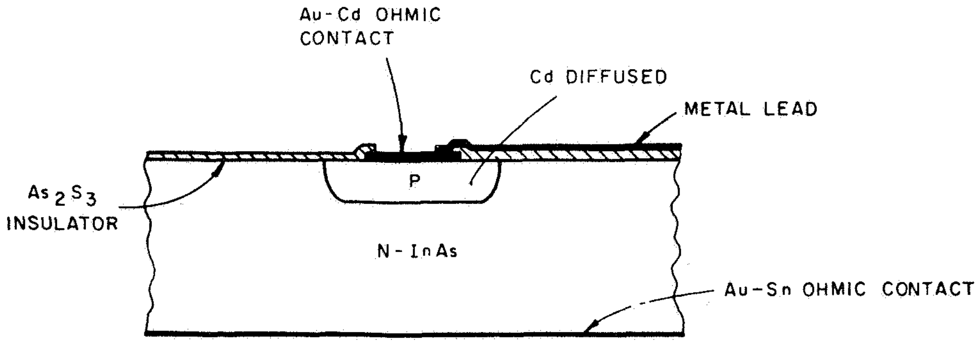


Figure 19. Cross-section of a Completed Planar Array Element

The V-I characteristics of the diode elements of the array were measured by probing the evaporated leads. A typical characteristic of a diode element is shown in Figure 21. It is seen that the diode is quite leaky and the sensitivity is not that good. This may be attributed to the fact that since the same mask was used for the ohmic contact and the opening through the As_2S_3 film, the metallized thin-film leads may make contact to the diffused surfaces.

Many attempts were made to improve the device characteristic and detector sensitivity of the array fabricated by this planar process. But the process has been so tedious and complex that we have not been able to obtain a planar process that gives a uniform and acceptable sensor array. Therefore, we have attempted to develop a different technique for array fabrication. This process is quite simple and yet the diode characteristic and optical sensitivity are far better than those of the array processed by the planar technique. The new processing steps will be discussed in the next section.

3. Delineated Array Process

The finalized array processing technique has been found to be relatively simple and straightforward, having a minimum number of critical steps. This process is identical to that described in the previous sections, through the diffusion processes. After diffusion, ohmic contacts are applied to the diffused diodes and the entire surface cleaned, using the same procedure previously described. The duration of this surface cleaning process was found to be an important control for the device leakage current. The array diodes with ohmic contact are shown in Figure 22.

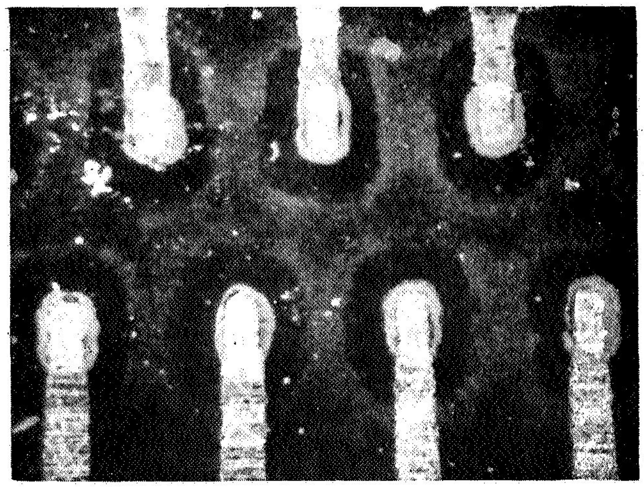


Figure 20. Typical Top View of a Completed Planar Array

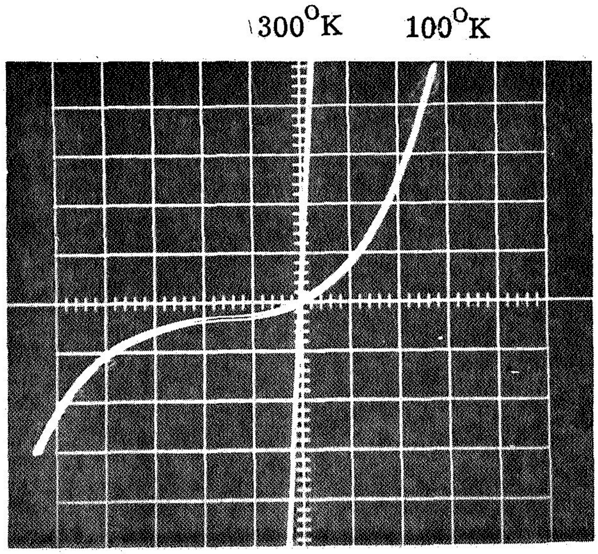


Figure 21. Typical V-I Characteristic of a Diode Element in the Planar Array Shown in Figure 20. (Scale:V = 10 μa/div. H = 0.1 volt/div.)

A basic problem encountered in the fabrication of high density arrays of InAs is the interconnection of the detector elements to the external electronic circuits. Since the InAs, unlike silicon, does not have its native insulating oxide, an additional complication is associated with the fabrication of multi-element detector array of InAs sensors. Basically, the process of lead attachment follows the classical approach of direct connection of the leads to the detector elements in the array. A pulsed thermocompression ball bonder was used to bond one mil gold wire from the alloyed sensor elements to the fan-out circuit board. The process was lengthy, but the connections were excellent and quite reliable. A complete package of the wire bonded 50 leads InAs sensor array is shown in Figure 23.

The uniformity of sensor elements was measured qualitatively by observing the diode characteristics at room temperature, which were quite uniform. A typical diode characteristic of the array elements at room temperature is shown in Figure 24. Figure 25 shows its curve at 77°K. It is seen that the reverse saturation current is extremely small over a 25-volt range and the breakdown at 30 volts is very sharp. It should be noted that the device characteristics of the delineated InAs array detector elements are far better than those of the previous devices and that none of these features have previously been reported in the open literature.

More quantitative measurements of this array will be discussed and all the pertinent optical and electrical measurements will be included in the following section.

D. MEASUREMENTS OF THE InAs PHOTODETECTOR ARRAY

Measurements performed on the array elements, described in the previous section, are discussed in this section. Since the performance of the delineated array is far better than that of the planar array, the measurements for only the delineated arrays were made, except where otherwise noted.

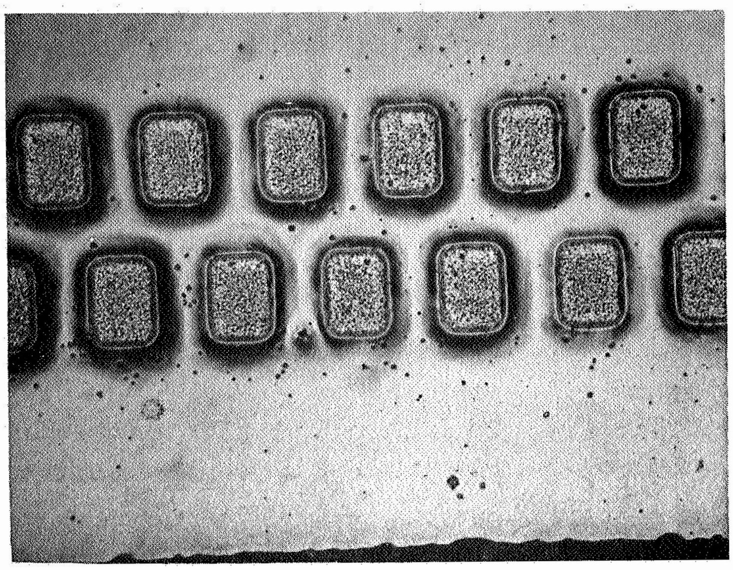


Figure 22. Delineated InAs Array

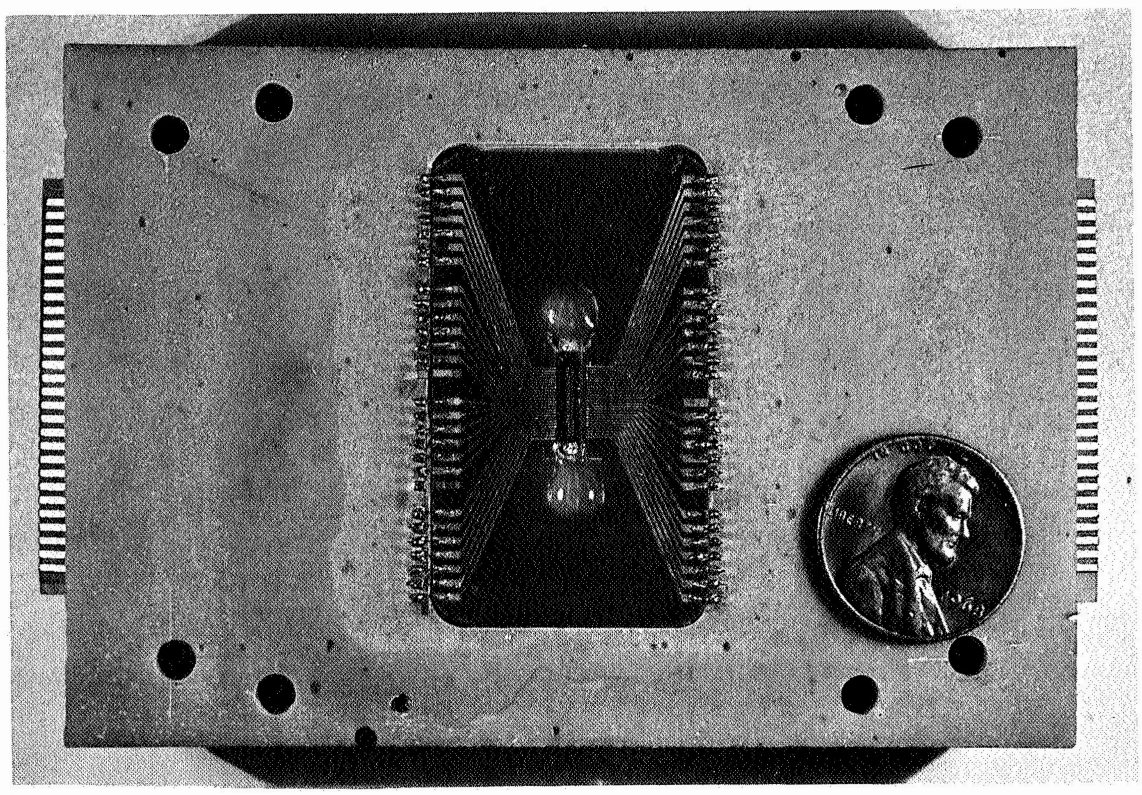


Figure 23. Wire Bonded Complete Package of InAs Array

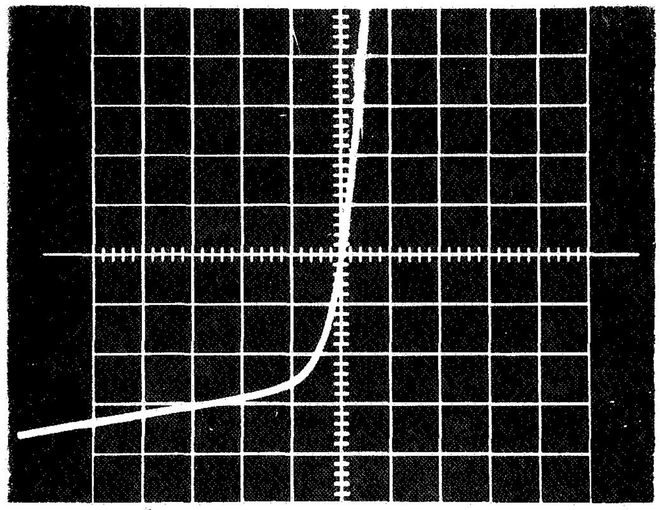


Figure 24. Diode Characteristic of a Typical Array Element at Room Temperature (V = 0.1 mA/div, H = 0.1 V/div.)

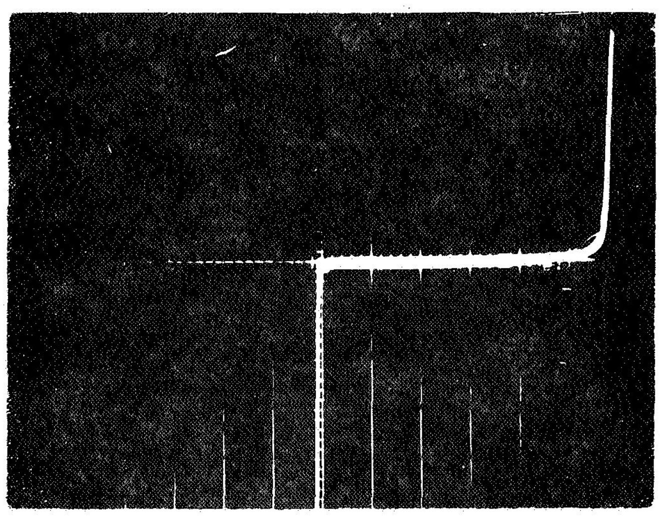


Figure 25. Diode Characteristic of a Typical Array Element at 100^{o}K (V = 10 μA/div., H = 5 V/div.)

1. Electrical Measurements

a. V-I Characteristics

The diode characteristics of an array element were measured accurately at both room temperature and $100^{\circ}K$. The characteristic at room temperature is shown in Figure 26. The dynamic resistance of the diode (R_d) was calculated from the slope of the curve at zero point; R_d = 270 ohms. At $100^{\circ}K$ it was difficult to measure the current at near zero voltage because of the extremely small current, but at higher voltages the measurements were made. The semi-log plot of the forward characteristic is shown in Figure 27. The value n is equal to one, indicating that no recombination of carriers takes place in the space-charge region of the junction. Figure 28 shows the characteristic in the reverse direction. It is seen that the leakage current of the diode is extremely small; less than one nanoamp up to the reverse bias voltage of 25 volts and a sharp breakdown occurs at 30 volts. It should be noted that the device characteristics of this type InAs diode are far better than previously reported and the low leakage nature of the diode is an excellent feature for sensitive infrared photodetector.

b. Noise Measurements

The noise measurements were performed using a Princeton Applied Research (PAR) Lock-in-Amplifier with type A preamp, a Hewlett Packard 302 Wave Analyzer, and a Ballantine 320 true RMS Volt Meter. The system frequency was determined by the tuned amplifier of the lock-in-amplifier with a Q of 10. The bandwidth of the wavelength analyzer was 6 cps.

Typical noise versus frequency for a large area planar device (see Figure 17) is shown in Figure 29. It is shown that the noise voltage follows the relation, $1/f^m$ where m = 1.4. The exact mechanism for this large excess noise generation in the diode is not fully understood at the present time. It appears, however, that the excess noise depends strongly on the surface of the diode. The large junction area diodes, which were made in the early phase of this program (see Section II. B), have always exhibited a current-controlled negative resistance type of breakdown. In some cases the diode voltage oscillates at breakdown. Typical V-I characteristic of such oscillation is shown in Figure 30.

One possible explanation for the negative resistance and oscillation is that small regions of the diode break down at a slightly lower voltage. Thus, the breakdown current does not pass uniformly through the junction over the entire junction area, but flows through the local junction regions causing

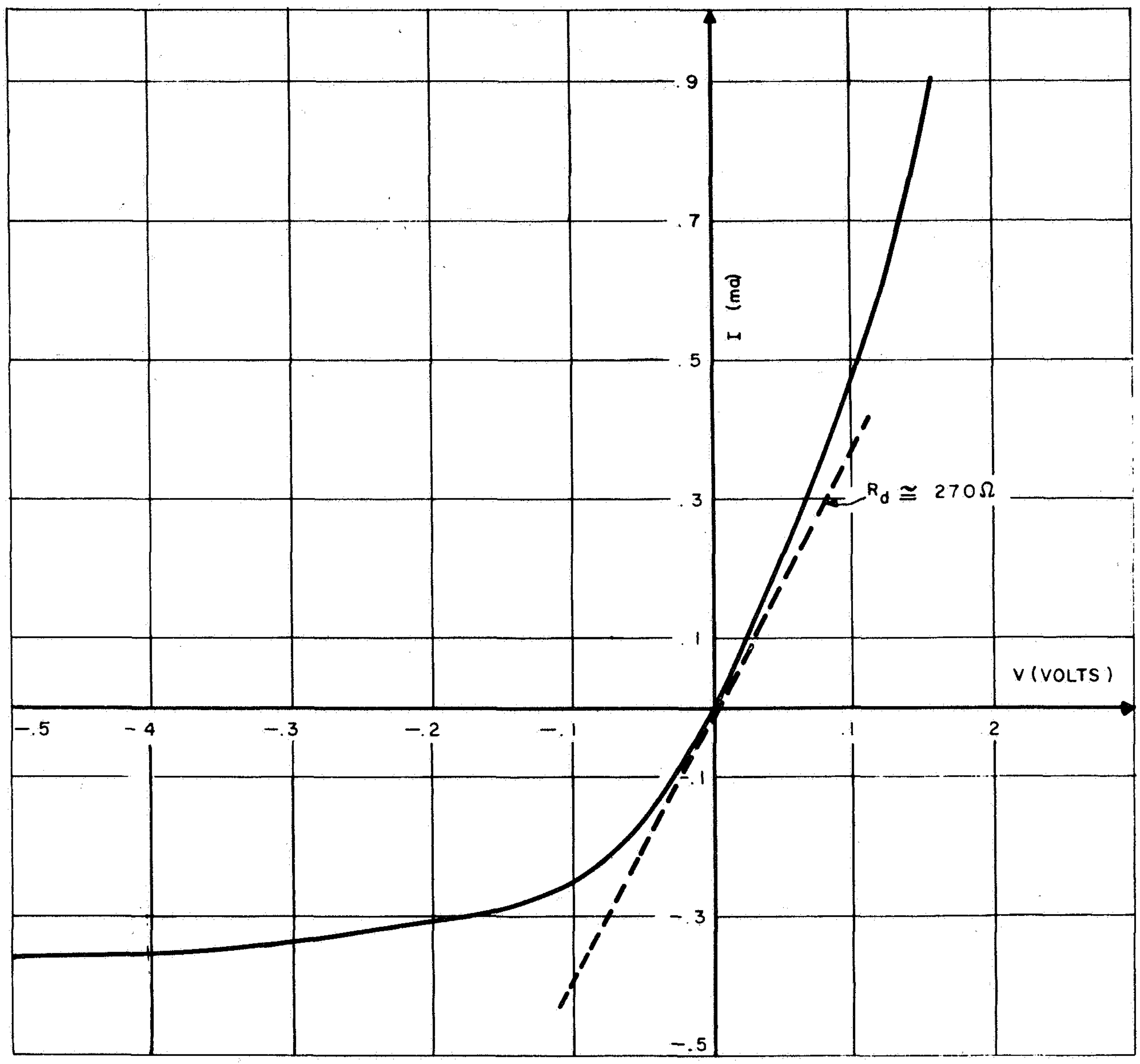


Figure 26. Typical Array Diode Characteristic
at Room Temperature

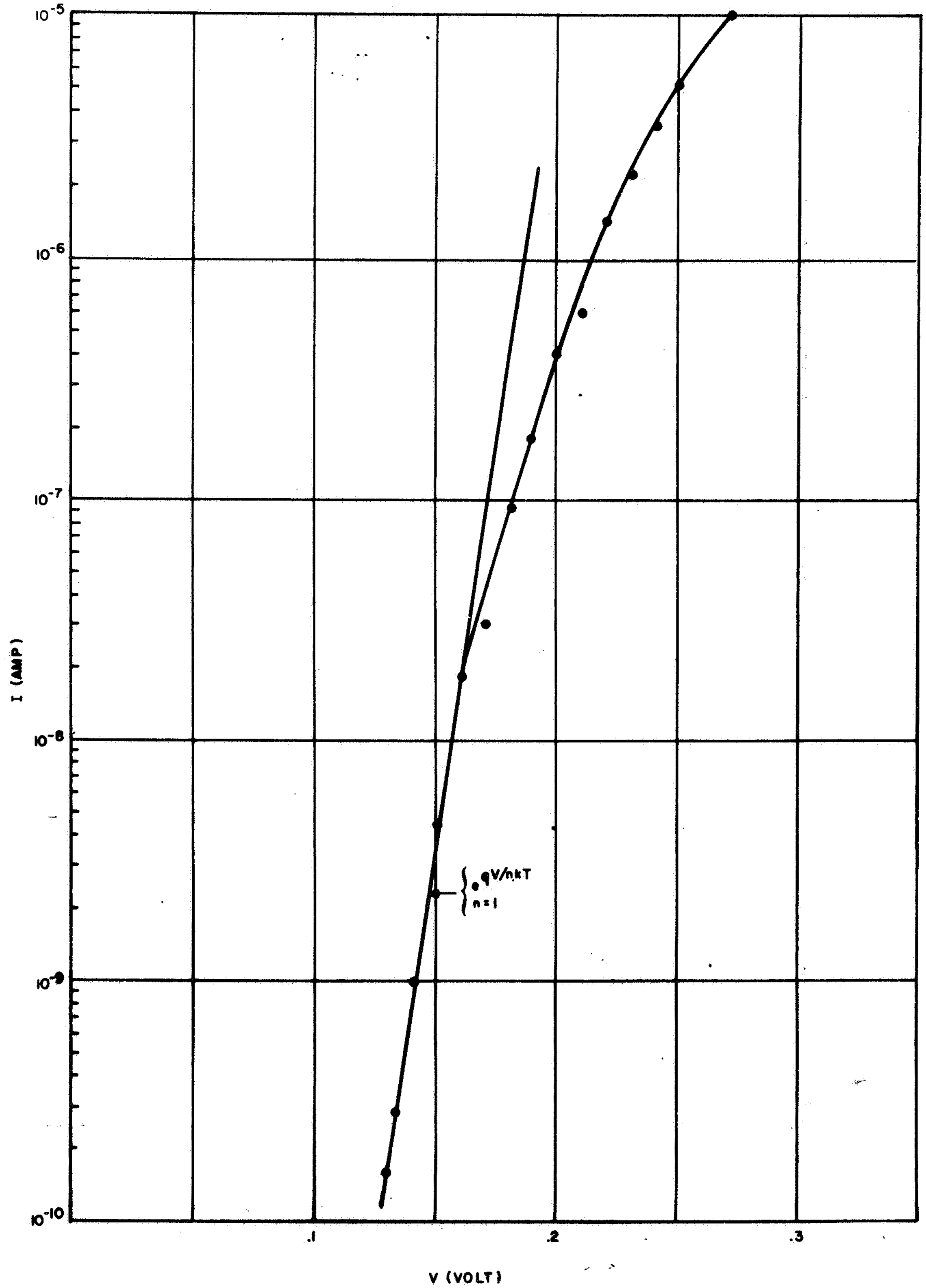


Figure 27. Forward Characteristic of a Typical Array Diode at 100°K

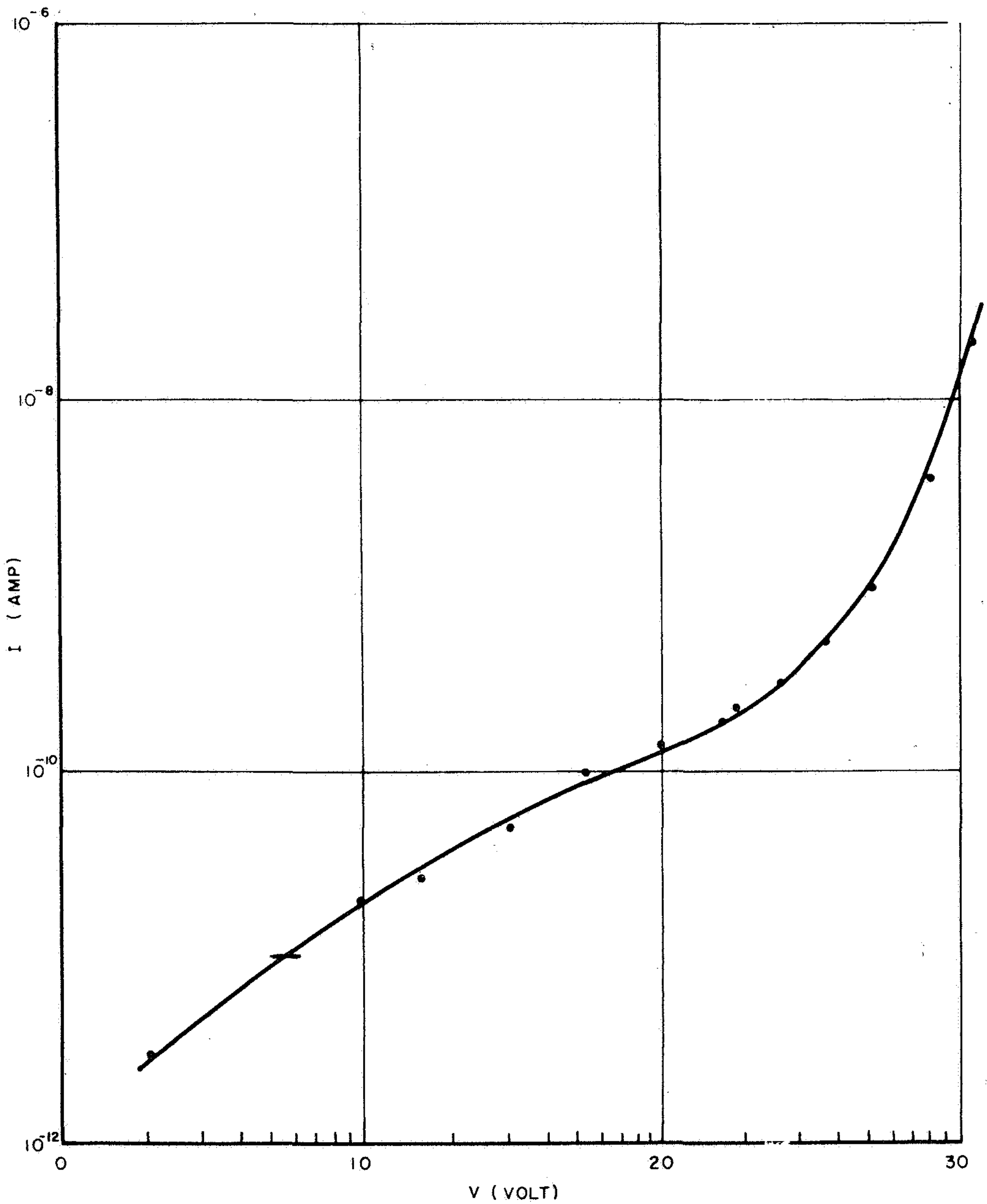


Figure 2. Reverse Characteristic of an Array Diode at $100^{O}K$

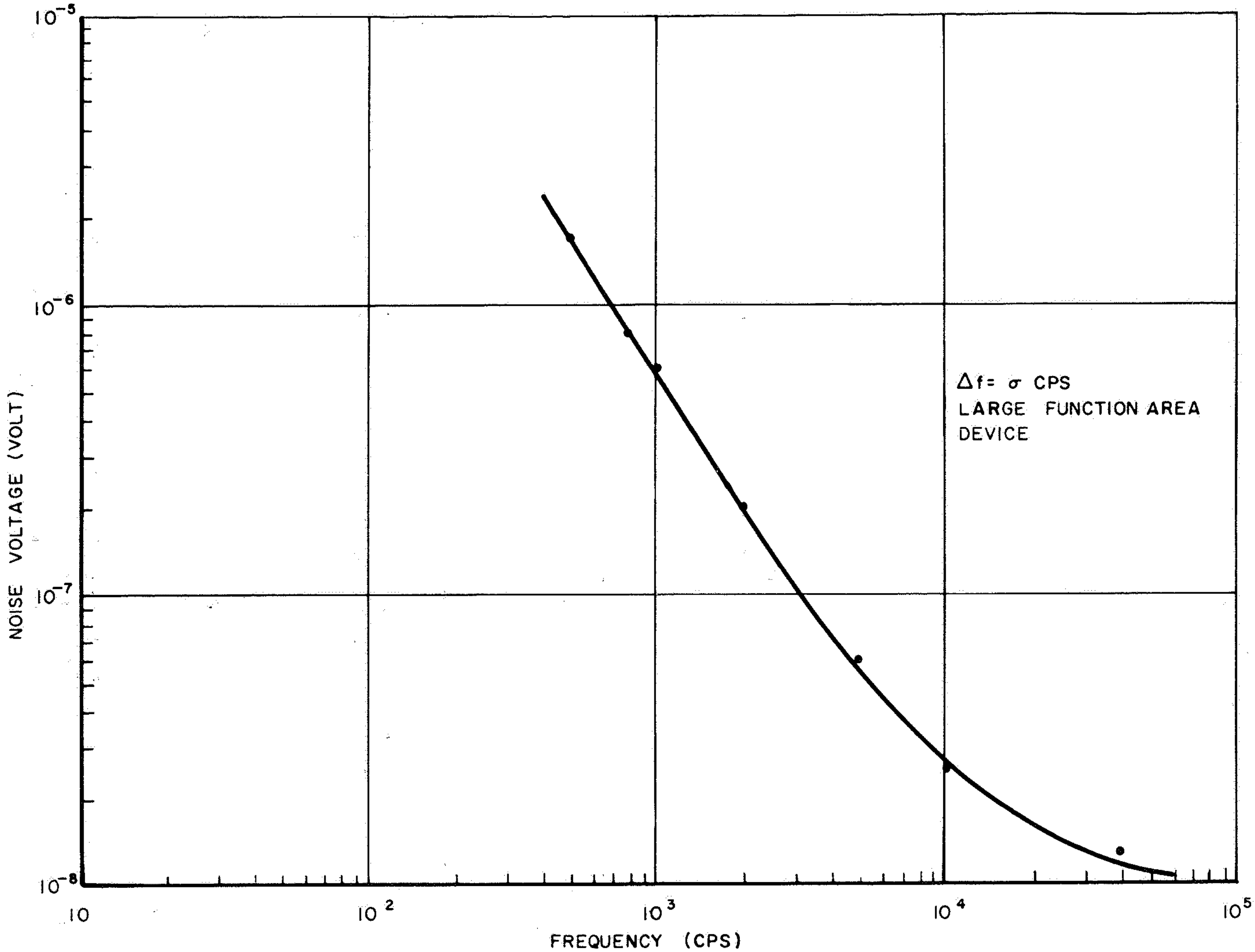


Figure 29. Noise Voltage as a Function of Frequency at $100^{\circ}K$ for Sample #34-A

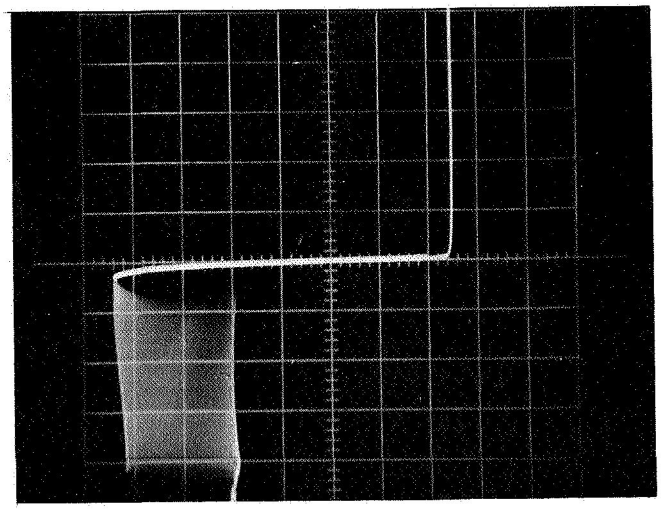


Figure 30. Typical Negative Resistance and Oscillation Characteristic of Large Area InAs Diode (Vertical: .05 ma/div.) Horizontal: .5 v/div.)

these regions to rise in temperature. This mechanism may be similar to the local breakdown spots that have been observed in silicon avalanche diodes, so-called microplasmas.

It has been observed that the negative resistance and oscillation characteristics are not always the same, particularly after exposure of the diode in air, indicating that the premature breakdowns occur at different spots of the junction area. It has been also observed that the smaller junction area diodes such as the array elements have not exhibited either negative resistance or any oscillations. The noise characteristic for the array elements as shown in Figure 31 is quite different from that of the large junction area diodes and shows little or no excess noise. Therefore, it seems that the large junction area devices are more vulnerable to the excess noise than the smaller junction diodes, and that the excess noise is directly related to the negative resistance and oscillation; to reduce the excess noise, the diode should not exhibit negative resistance or oscillation.

The above noise voltage of an array element photovoltaic diode will be used in the following section to determine the noise-equivalent-power (NEP) or D* from the responsivity measurements, which is discussed in the next section.

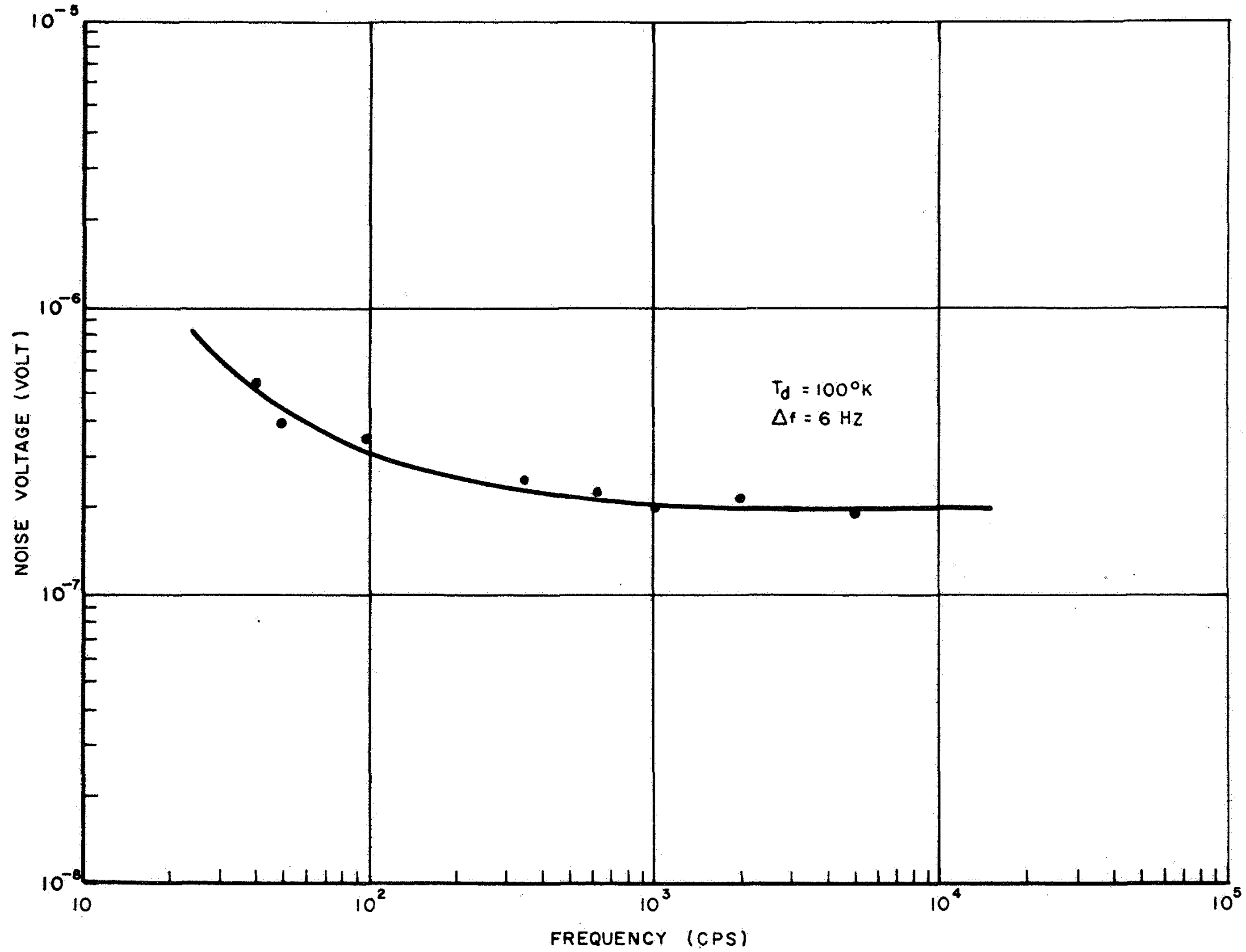


Figure 31. Noise Voltage versus Frequency for an Array Element Detector

2. Optical Measurements

The optical measurements were carried out using a blackbody source, a synchronous variable speed chopper, and lock-in amplifier. Figure 32 illustrates the typical setup for the optical measurements. For spectral measurements, accurately calibrated filters were used. For room temperature detector measurements ($T_d = 300^oK$), the blackbody source temperature was set at 800^oC ($T_b = 800^oC$). For 100^oK detector measurements ($T_d=100^oK$), the blackbody source temperature was set at 300^oC. ($T_b = 300^oC$). The photovoltaic signals were measured as a function of the radiation intensity, the chopping frequency, and wavelength for room temperature and 100^oK. Finally, the detectivity D* was obtained from these measurements and the noise measurements discussed in the previous section.

The photoresponse as a function of the blackbody radiation was measured in order to see the range of the linear region. The results are shown in Figure 33. The radiation intensity on the detector surface was varied by adjusting the position of the detector with respect to the blackbody source with constant source temperature. It is seen that at 100^oK the output voltage of the detector is saturating above about 3 mv, and below this point the curve is quite linear. In the previous report we have shown that the photon generated excess minority carriers at junction = $n_o e^{\beta V}$, where n_o is the equilibrium minority carrier density, V is the output voltage, and $\beta = q/kT$. At $T = 100^oK$, $1/\beta$ = 8.63 mv. If the generated voltage, V, is much smaller than $1/\beta$, an approximation can be made and the voltage is directly proportional to the excess minority carriers; that is, to the radiation intensity as shown in the figure. Therefore, in order to operate the InAs photovoltaic detector in the linear region, the output signal voltage should be below a few millivolts. The signal level of a practical InAs infrared detector is usually much smaller than these voltages and thus no non-linearity will occur in typical application. At room temperature, the signal voltage is linear with the intensity even though the blockbody temperature was raised up to 800^oC.

The signal voltages were measured as a function of the chopping frequencies for both room temperature and 100^oK as shown in Figure 34. At 100^oK, the signal is 3 dB down at around 1,200 Hz, whereas the signal at room temperature is constant with the chopping frequency. This is attributed to the fact that at lower temperatures, the diode impedance is so large that the detector becomes RC limited. As shown in Figure 26, the diode impedance at room temperature was about 270 ohms, whereas at 100^oK the diode dynamic resistance was so high that it was difficult to measure. This indicates that at low temperature the photovoltaic mode of operation may not be recommended for high-speed application. However, typical operating temperature of InAs detectors is much higher than 100^oK and therefore a higher speed would be expected. Furthermore, since the diode leakage current is extremely small, the reverse bias photodiode appears to be quite promising for high-frequency application.

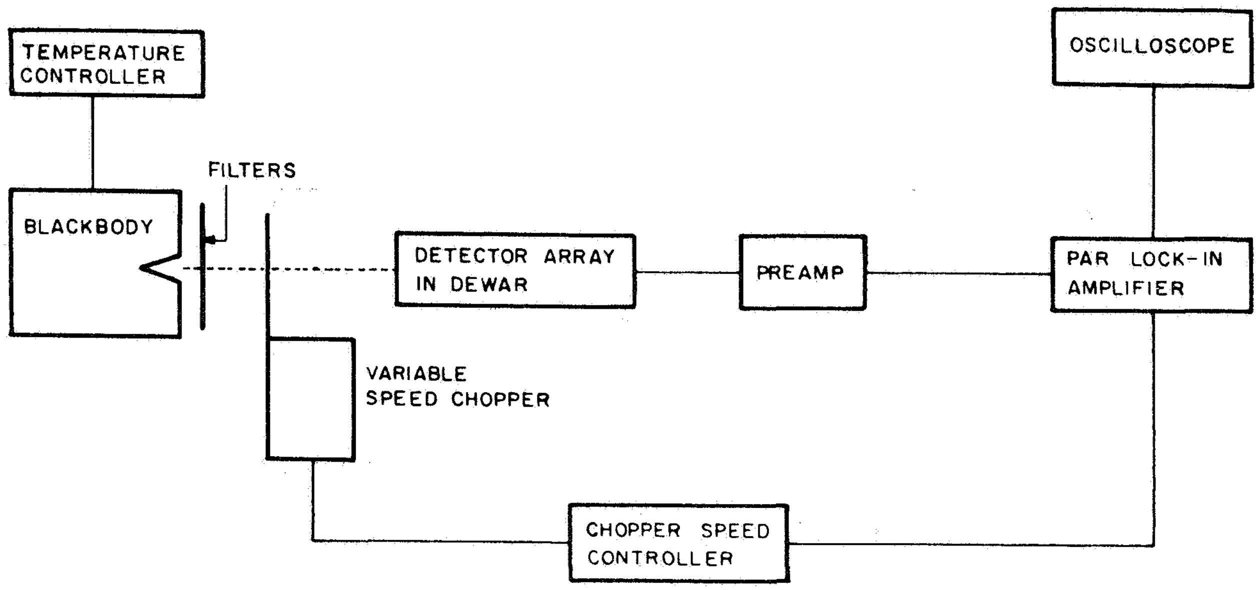


Figure 32. Optical Measurement Setup

The spectral response measurements of a typical array element were performed using calibrated filters and a blackbody source. At a detector temperature of 100°K, the blackbody temperature was set at 300°C. For room temperature measurements, a source temperature of 800°C was used in order to increase the signal level. Figure 35 shows the responsivity versus wavelength for the two temperatures. The responsivity is defined by the signal voltage divided by the optical power signal (volts/watt). It is seen that at room temperature the peak is at about 3.5 microns and at 100°K, the peak occurs at 3.1 microns. These results agreed with the available data. Thus, it is insured that the array elements respond properly to the wavelength. The total blackbody responsivities are

$$R_{bb} = 1.4 \times 10^2 \text{ volts/watt for } T_d = 300^\circ K$$

$$R_{bb} = 2.3 \times 10^5 \text{ volts/watt for } T_d = 100^\circ K.$$

D* versus wavelength at 100°K and 300°K is shown in Figure 36. D*'s were calculated from the responsivity and noise measurements;

$$D^* = \frac{\sqrt{A_d}}{\frac{V_n}{\sqrt{\Delta f}}} \text{ (Responsivity)}$$

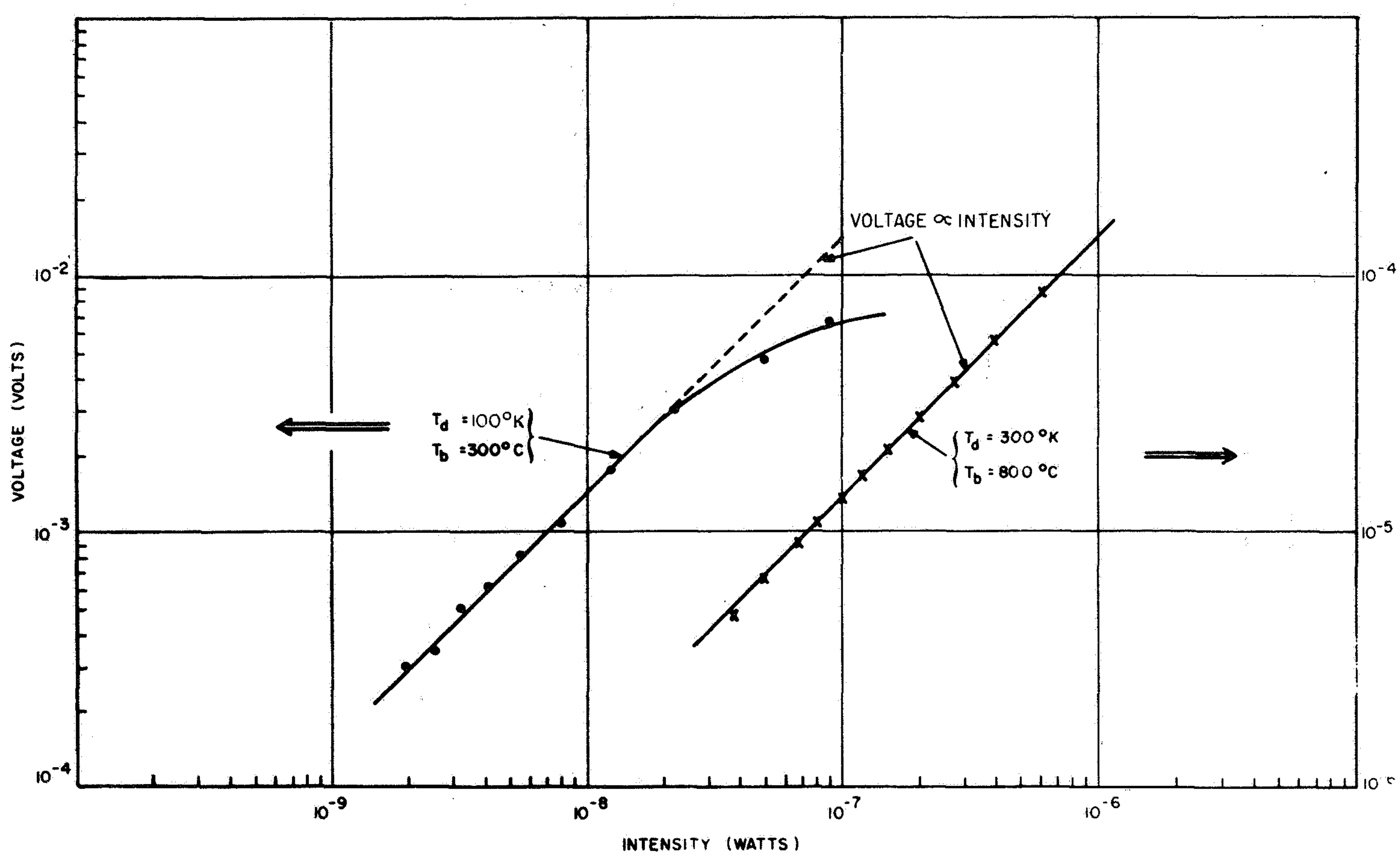


Figure 33. Photoresponse versus Radiation Intensity (T_d = detector temperature; T_b = blackbody temperature)

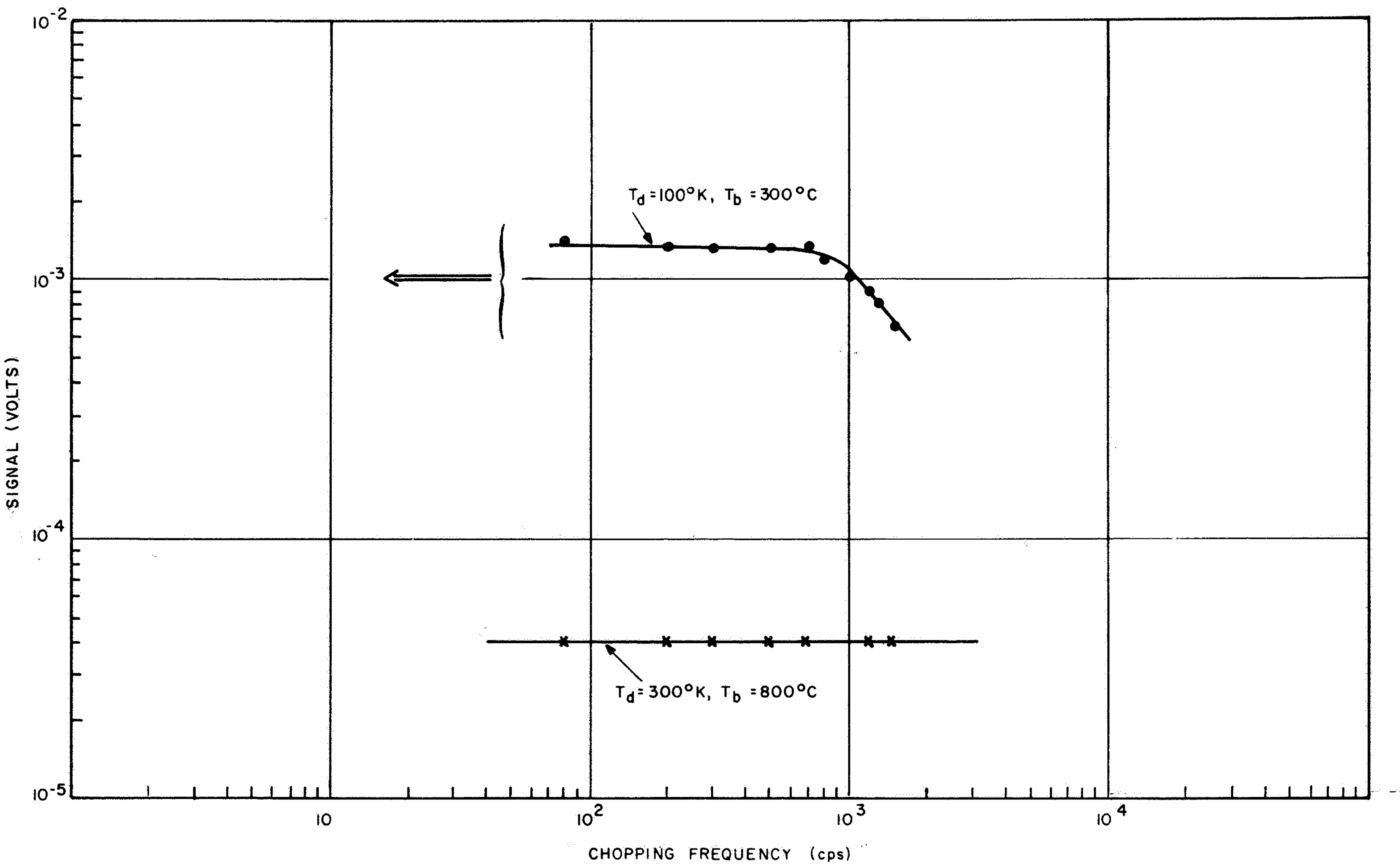


Figure 34. Signal Voltage versus Chopping Frequency

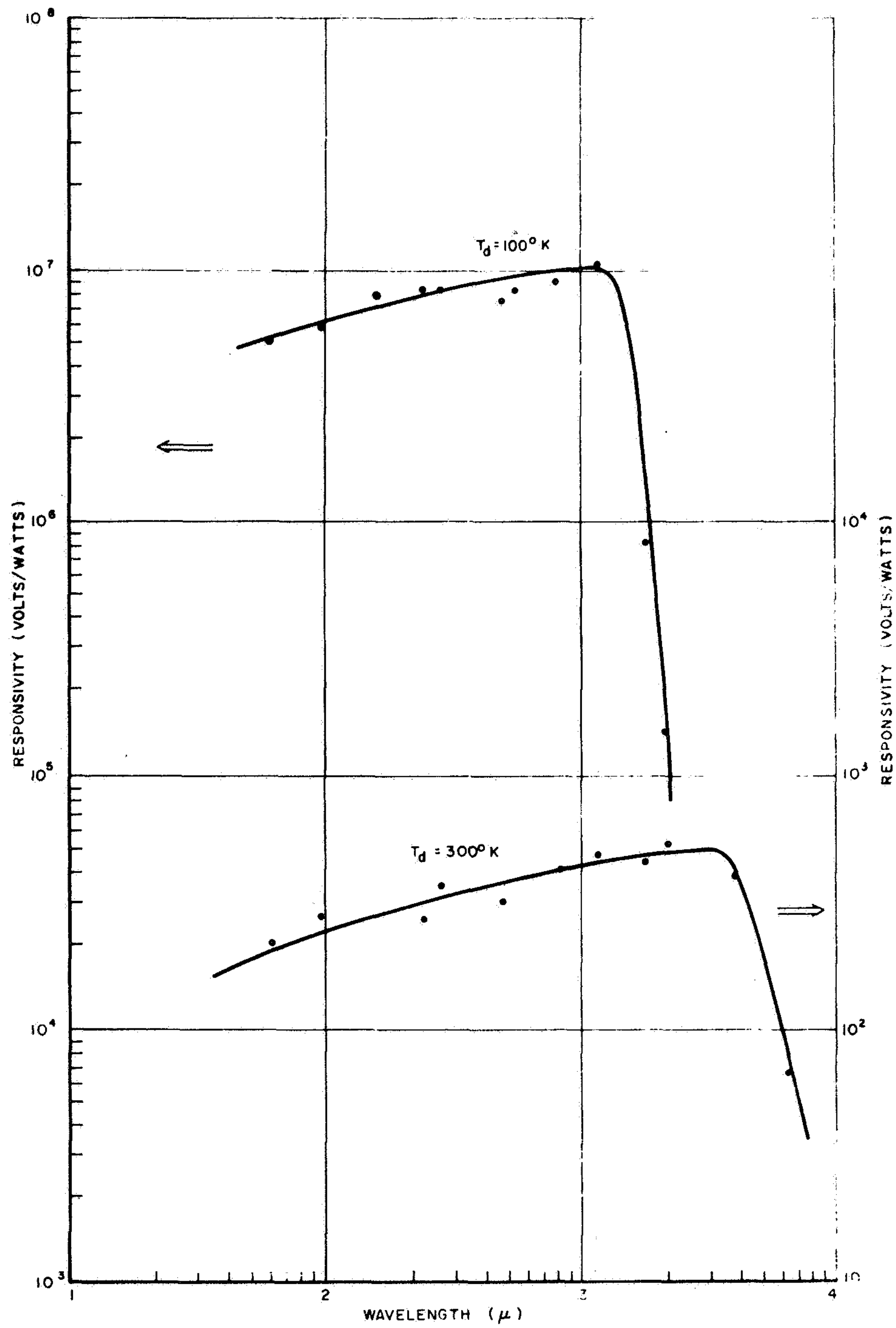


Figure 35. Spectral Response

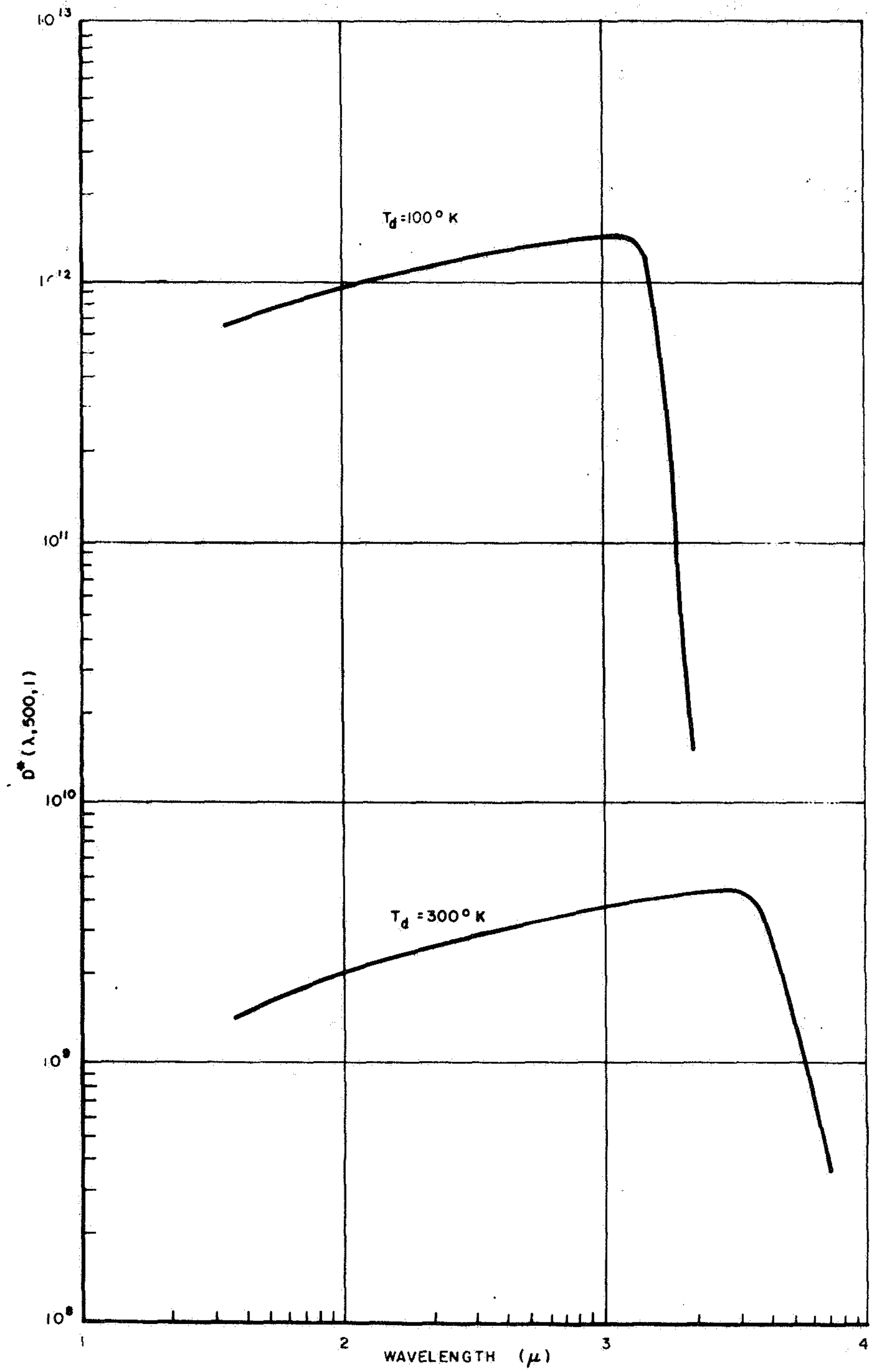


Figure 36. D* Versus Wavelength

where $A_d = 1.8 \times 10^{-4}$ cm^2, at $T_d = 100^oK$ $V_n = 2.2 \times 10^{-7}$ volts for $\Delta f = 6$ Hz, and at $T_d = 300^oK$ $V_n = 1.5 \times 10^{-9}$ volts for $\Delta f = 1$ Hz. The blackbody D^*_{bb}'s are

$$D^*_{bb}\ (800^oC,\ 500,\ 1) = 1.25 \times 10^9 \text{ cm Hz}^{\frac{1}{2}}/\text{watt for } T_d = 300^oK$$

$$D^*_{bb}\ (300^oC,\ 500,\ 1) = 3.5 \times 10^{10} \text{ cm Hz}^{\frac{1}{2}}/\text{watt for } T_d = 100^oK.$$

3. Uniformity of the Array Elements

The uniformity of the array elements was measured under the following test conditions:

Blackbody temperature	= 500°C
Array temperature	= -100°C
Distance to Array	= 9.0 inches
Noise Bandwidth	= 6.0 Hz
Blackbody aperture	= 0.2 inches diameter

The results were calculated and tabulated using a computer, and the computer print out is reproduced in Table VI. The data are plotted in Figure 37. The average values for the detector elements in this array are

$$\text{Average } D^*_{bb} = 1.1 \times 10^{11} \text{ cm (HZ)}^{\frac{1}{2}}/\text{watt}$$

$$\text{Average Responsivity} = 2.4 \times 10^5 \text{ volts/watt}$$

The distribution of values of D* for the elements are tabulated below:

Spread	% of Elements Within Spread
± 50%	98%
± 30%	92%
± 20%	76%
± 10%	40%

It appears that the cause of non-uniformity of the array elements is attributed to the direct wire bonding to the detector elements. Different detector geometry and wire bonding technique will improve the array uniformity.

4. Isolation Measurement

The isolation of the elements in the array was determined by illuminating the array with a .040 spot and measuring the signal measured at each diode in the array. The results, shown in Figure 38, demonstrate that each element is independent. As the spot of light is moved from element to

TABLE VI.

D* AND RESPONSIVITY FOR ARRAY 56-2-P2

ARRAY ELEMENT NUMBER	RMS SIGNAL VOLTAGE VOLTS	RMS NOISE VOLTAGE VOLTS	D* DETECTIVITY CM*SQRT(HZ)/WATT	RESPONSIVITY VOLTS/WATT
1	3.600E-03	6.000E-08	1.169E+11	[illegible]
2	3.600E-03	6.000E-08	1.169E+11	[illegible]
3	3.600E-03	6.000E-08	1.169E+11	[illegible]
4	3.600E-03	6.000E-08	1.169E+11	[illegible]
5	3.700E-03	6.000E-08	1.202E+11	2.11[illegible]
6	3.700E-03	6.000E-08	1.202E+11	2.11[illegible]
7	3.700E-03	6.000E-08	1.202E+11	2.11[illegible]
8	3.400E-03	6.000E-08	1.104E+11	1.946E+05
9	3.500E-03	7.000E-08	9.744E+10	[illegible]
10	3.300E-03	6.000E-08	1.072E+11	[illegible]
11	3.700E-03	6.400E-08	1.127E+11	2.116E+05
12	3.[illegible]00E-03	6.600E-08	1.234E+11	2.175E+05
13	4.200E-03	6.400E-08	1.279E+11	2.404E+05
14	4.200E-03	[illegible]	1.023E+11	2.404E+05
15	4.200E-03	[illegible]	9.961E+10	2.4[illegible]E+05
16	7.600E-03	2.000E-07	7.405E+10	4.35[illegible]E+05
17	8.500E-03	2.[illegible]E-07	[illegible]	4.865E+05
18	9.600E-03	1.[illegible]E-07	1.[illegible]39E+11	5.494E+05
19	9.600E-03	2.[illegible]E-07	9.354E+10	5.494E+05
20	[illegible].600E-03	2.300E-07	7.267E+10	4.9[illegible]E+05
21	6.000E-03	1.[illegible]E-07	1.169E+11	3.434E+05
22	4.600E-03	7.[illegible]E-08	[illegible].994E+10	2.2[illegible]E+05
23	3.800E-03	[illegible]	9.257E+10	2.175E+05
24	3.700E-03	7.000E-08	1.082E+11	2.[illegible]E+05
25	3.200E-03	6.[illegible]E-08	1.[illegible]39E+11	1.831E+05
26	3.290E-03	5.[illegible]E-08	1.247E+11	1.831E+05
27	3.400E-03	5.[illegible]E-08	1.325E+11	1.946E+05
28	3.400E-03	5.400E-08	1.227E+11	1.946E+05
29	3.300E-03	5.600E-08	1.148E+11	1.889E+05
30	3.600E-03	5.4[illegible]E-08	1.229E+11	2.0[illegible]E+05
31	3.500E-03	5.400E-08	1.2[illegible]3E+11	2.00[illegible]E+05
32	3.500E-03	5.000E-08	1.364E+11	2.[illegible]3E+05
33	3.700E-03	5.600E-08	1.2[illegible]E+11	2.11[illegible]E+05
34	3.700E-03	5.600E-08	1.2[illegible]E+11	2.11[illegible]E+05
35	3.500E-03	5.600E-08	1.216E+11	2.0[illegible]E+05
36	3.500E-03	5.[illegible]00E-08	1.21[illegible]E+11	2.003E+05
37	3.600E-03	5.600E-08	1.253E+11	2.[illegible]E+05
38	3.4[illegible]E-03	5.600E-08	1.183E+11	1.946E+05
39	4.100E-03	5.600E-08	1.427E+11	2.346E+05
40	4.[illegible]E-03	6.000E-08	1.299E+11	2.[illegible]E+05
41	4.300E-03	1.000E-07	[illegible].35[illegible]E+10	2.461E+05
42	3.[illegible]E-03	1.000E-07	7.465E+10	[illegible].17[illegible]E+05
43	3.200E-03	7.000E-08	8.909E+10	1.[illegible]31E+05
44	5.[illegible]E-04	6.000E-08	1.024E+10	2.[illegible]E+04
45	[illegible]E-03	9.000E-08	1.343E+11	[illegible]
46	5.[illegible]E-03	9.000E-08	1.126E+11	2.[illegible]E+05
47	4.000E-03	8.000E-08	9.744E+10	2.289E+05
48	4.000E-03	8.000E-08	9.744E+10	2.259E+05
49	3.600E-03	9.000E-08	7.795E+10	2.060E+05
50	2.[illegible]E-03	6.000E-08	8.445E+10	1.4[illegible]E+05

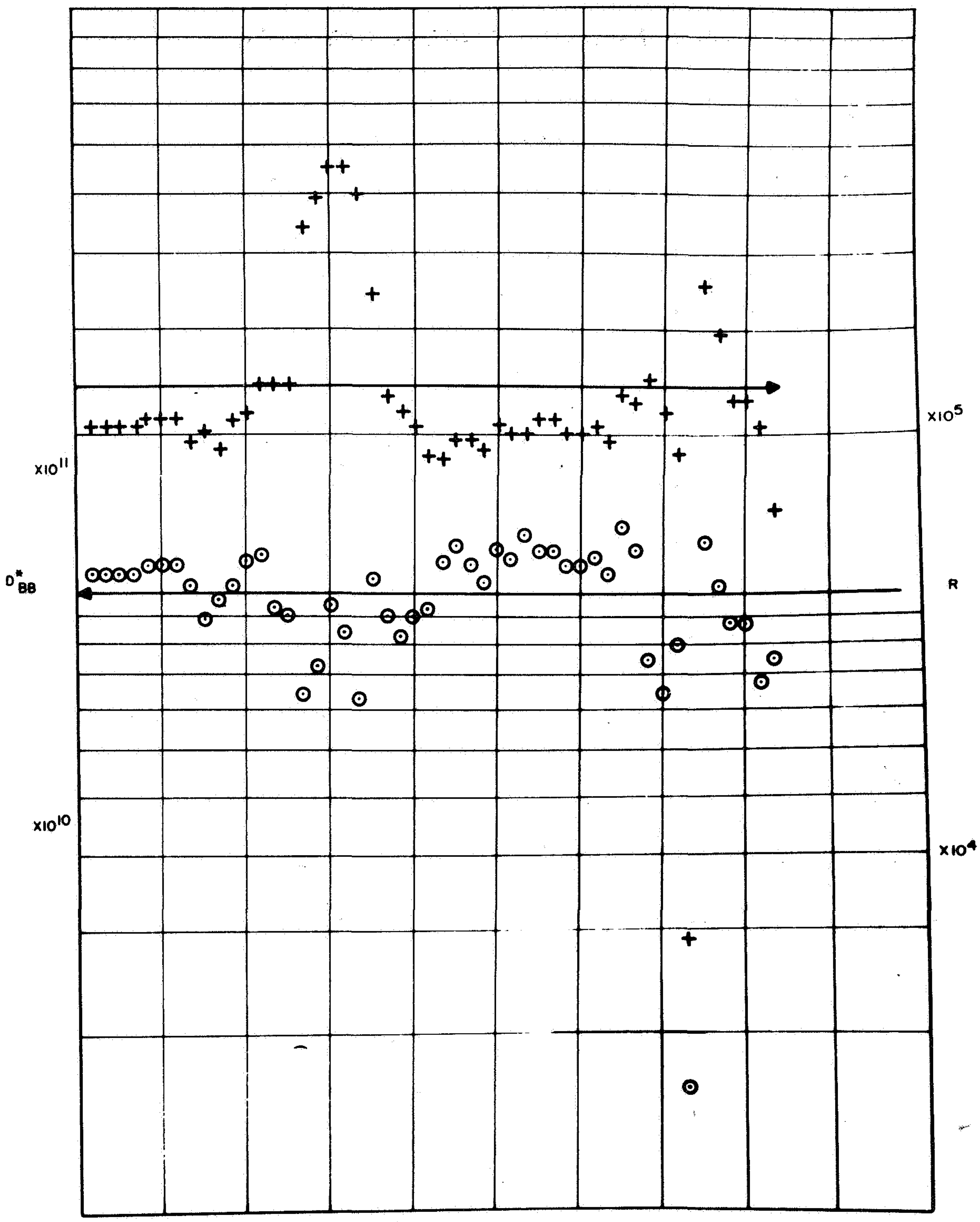


Figure 37. Data Plot, Array Element Uniformity

element, the corresponding photovoltage increases to the peak value, as indicated by the three curves in the figure. Although it was not an intended output of this measurement, the approximate linearity of the diode is indicated by the curve.

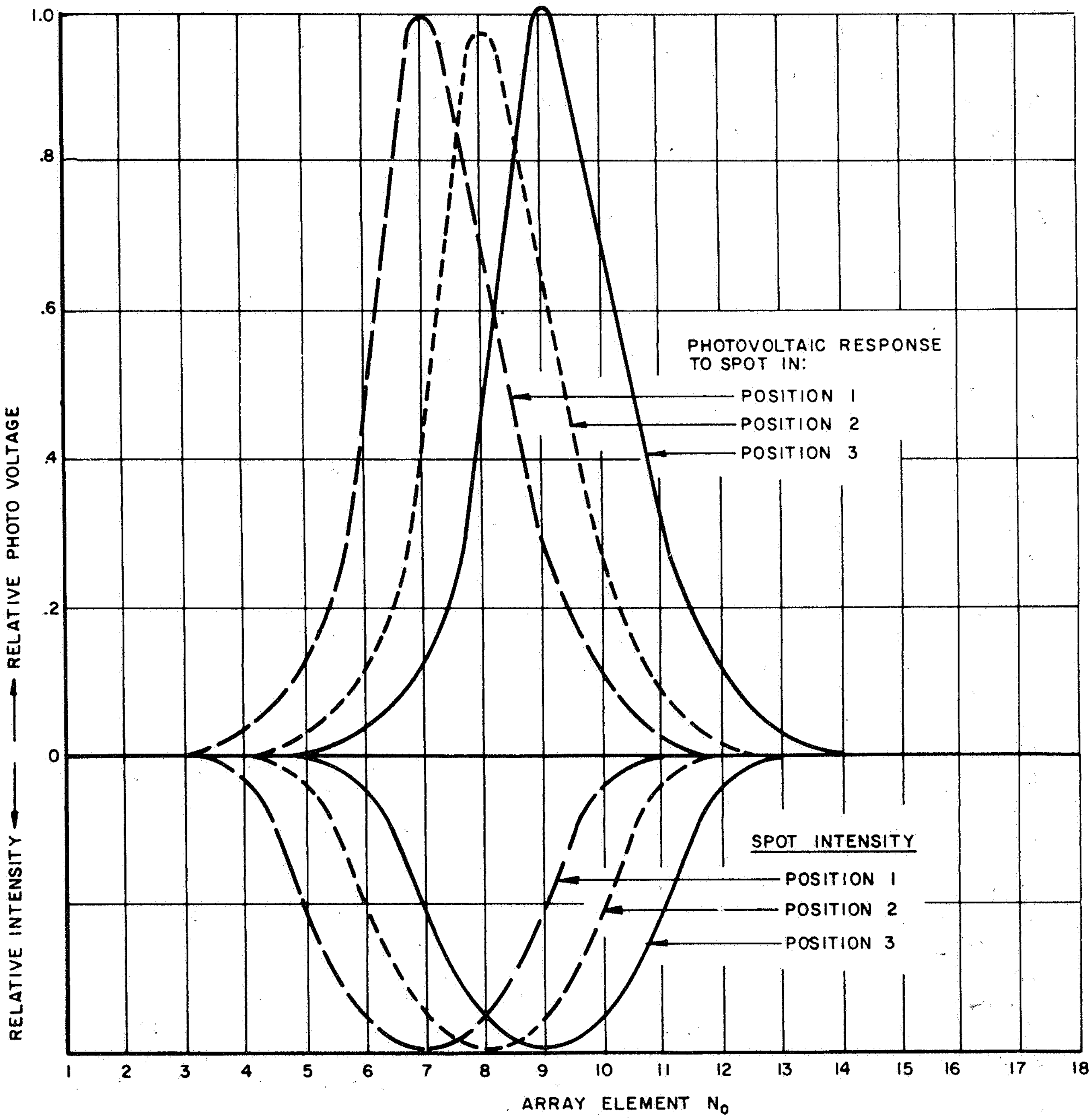


Figure 38. Array Element Isolation Measurement Results

III. PbSnTe DETECTORS

As a task under the Solid State Image Sensor Research Program, long-wavelength detectors were evaluated. One material, PbSnTe, was selected for detailed study and evaluation. In addition, during this same time period, the General Electric Electronics Laboratory carried out an independent materials development for PbSnTe. For the sake of completeness, much of this work is reported in this section.

A. PbSnTe DETECTOR MATERIALS

1. Crystal Growth

It has been known for some time that the binary compounds, PbTe and SnTe, form a continuous series of solid solutions of the general formula, $Pb_{1-x}Sn_xTe$. We have grown single crystals of $Pb_{1-x}Sn_xTe$, with x in the range of 0. 1 to 0. 2, employing the Bridgman technique.

A variety of parameters are important for the successful growth of single-crystal $Pb_{1-x}Sn_xTe$. In order to achieve a low density of imperfection, and to avoid the formation of spurious nucleation, the radial temperature gradient must be kept to a minimum. The axial gradient is a compromise between the low vacancy condensation and elimination of constitutional supercooling. A Marshall furnace, with a modified temperature profile, was used to grow single-crystal $Pb_{1-x}Sn_xTe$ by slowly lowering the melt through a sharp temperature gradient (see Figure 39). Marked changes in mechanical properties (e. g., brittleness of the wafers) were noticed at different drop rates. A slow drop rate is necessary in order to avoid disproportionation of the alloy. In addition, more homogeneous and less brittle crystals are obtained by further decreasing the drop rate. Ingots of $Pb_{x-1}Sn_xTe$, 7mm and 12mm in diameter and 2 to 5 cm long have been obtained, (see Figure 40). Laue x-ray diffraction experiments show a well defined single crystal pattern (Figure 41). Usually the crystals grow on the (100) plane of the NaCl crystal structure. In some cases, there is evidence of strain and twinning. The composition of the alloy was determined from x-ray analysis, assuming that Vegard's law applies. The crystals were fairly pure and homogeneous. No trace of anything other than $Pb_{1-x}Sn_xTe$ was detected. For x = 0. 2, the variation in x was 10%. The first-to-freeze portion was always rich in Pb, as shown in Figure 42. For a liquid composition of x = 0. 2, the first-to-freeze solid composition ranged between 0. 10 and 0. 14. Near the end of solidification, the maximum value of x was 0. 25. These facts indicate (1) incomplete mixing in the melt and (2) transport of the solid through the liquid by diffusion. We have found that it is indeed possible to grow large homogeneous ingots of $Pb_{1-x}Sn_xTe$, for various x values, using the Bridgman method, if the conditions for crystallization are properly chosen.

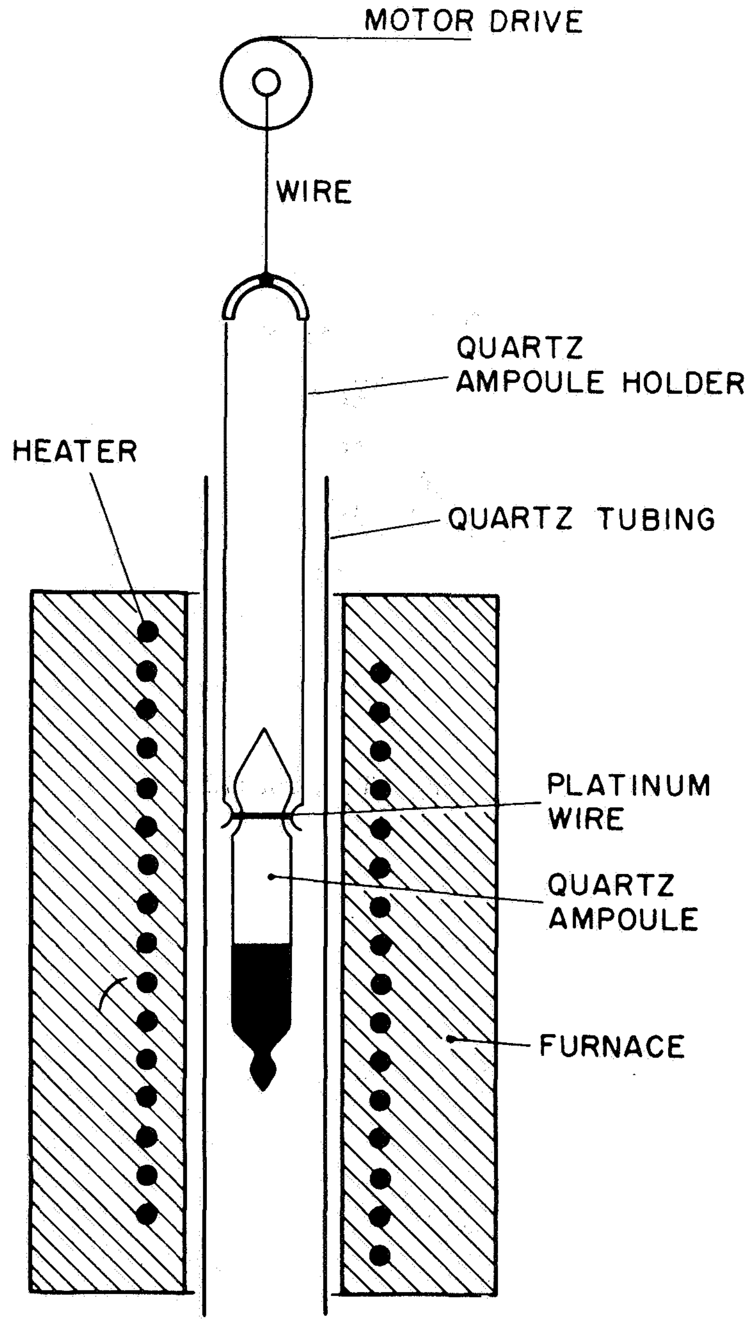
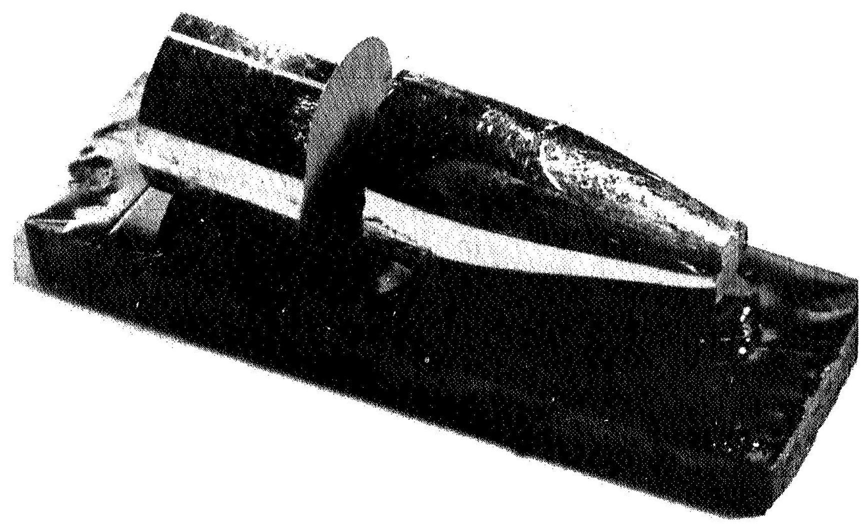
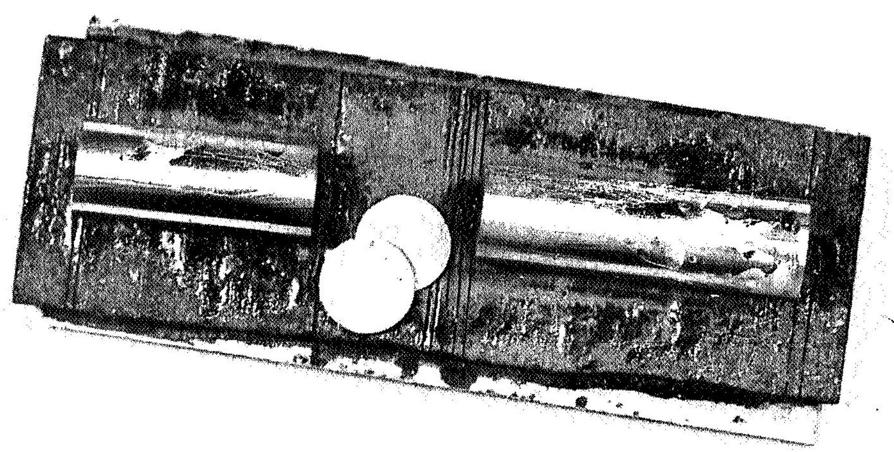


Figure 39. Marshall Furnace with Modified Temperature Profile



a. $Pb_{0.8}Sn_{0.2}Te$ Ingot (12 mm dia.)



b. $Pb_{0.8}Sn_{0.2}Te$ Ingot (7 mm dia.)
(Wafers Cut from Single-crystal Boule)

Figure 40. Photographs of Typical $Pb_{0.8}Sn_{0.2}Te$ Ingots

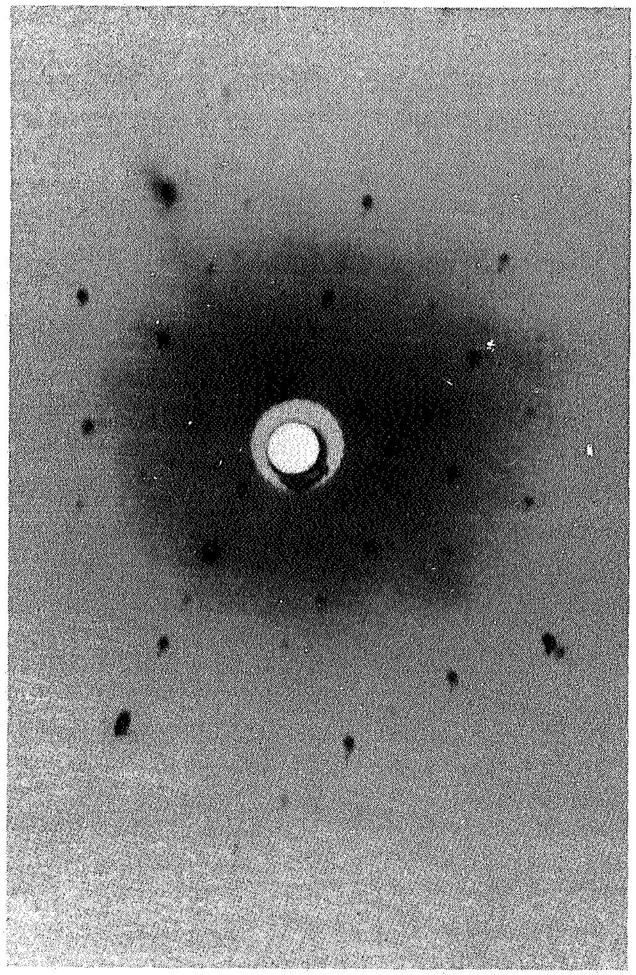


Figure 41. Laue X-ray Diffraction Showing Single-Crystal $Pb_{1-x}Sn_xTe$ Pattern

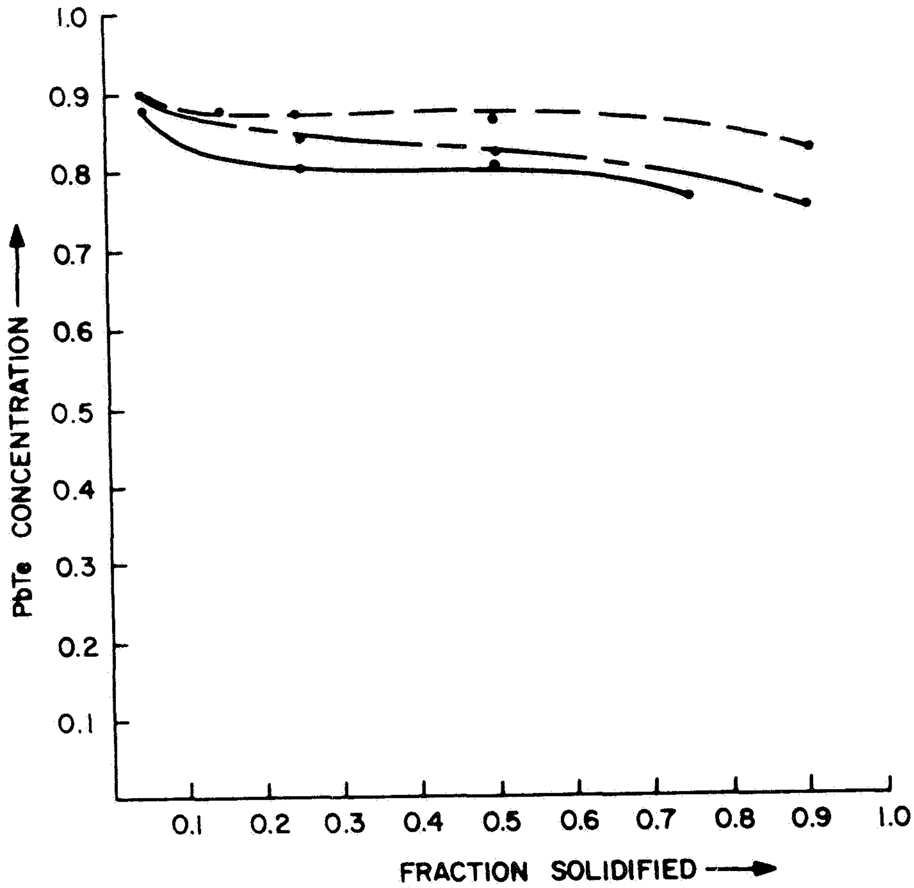


Figure 42. Distribution of PbTe in $Pb_{0.8}Sn_{0.2}Te$ Alloy

We have also grown reasonably large (several mm dimension) crystals of $Pb_{0.8}Sn_{0.2}Te$ by the vapor growth method (Figure 43). Depending upon the stoichiometry of the initial powder, it was possible to grow both n-and p-type crystals.

2. Electrical Measurements

Hall and resistivity measurements have been performed on several single-crystal samples. Figure 44 shows Hall coefficient values (in cm^3/coulomb) as a function of temperature for several different crystals. All of the samples were Bridgman-grown, p-type, and some were annealed to reduce carrier concentration, which at 77°K varied from $4 \times 10^{19}/cm^3$ (as grown) to $1.5 \times 10^{17}/cm^3$ (annealed).

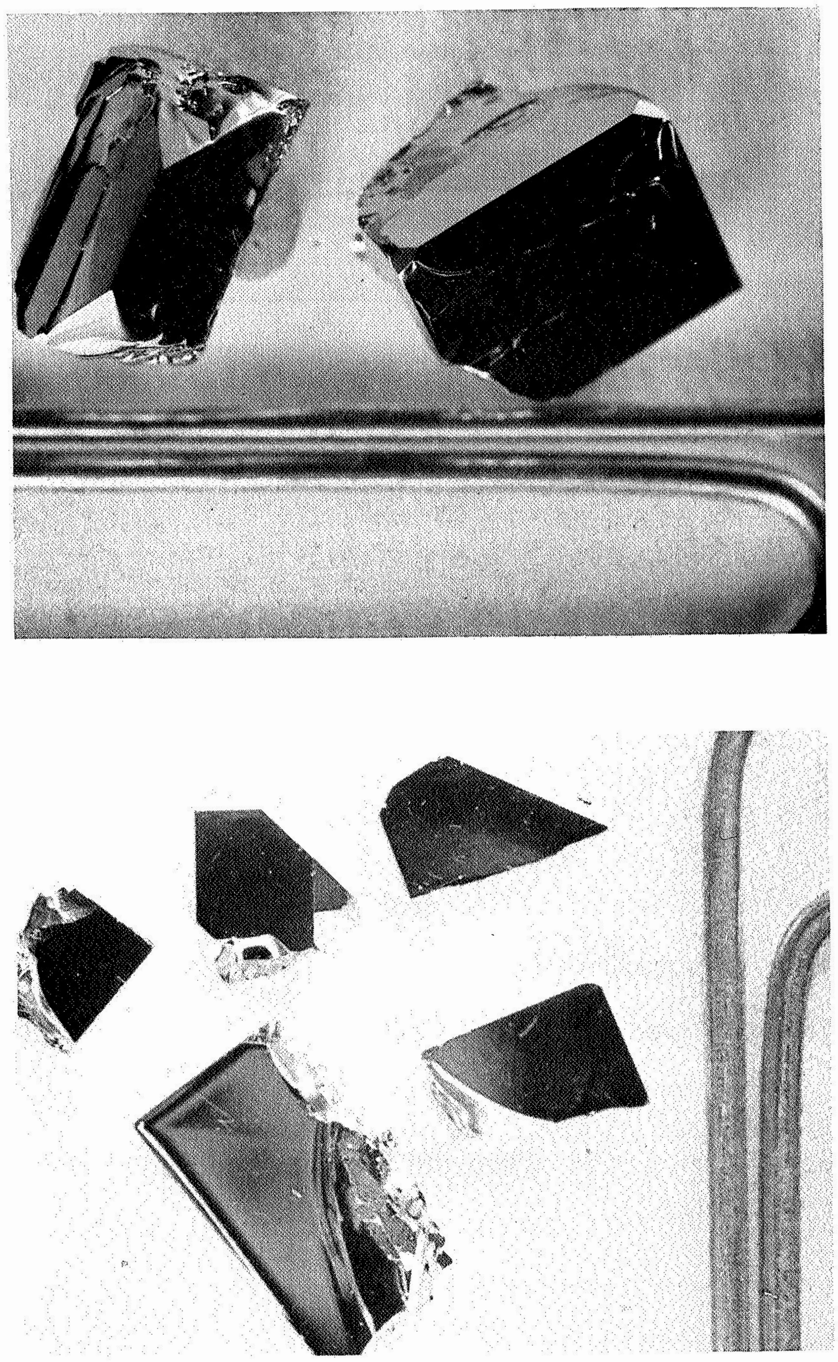


Figure 43. Vapor-grown Crystals of $Pb_{0.8}Sn_{0.2}Te$

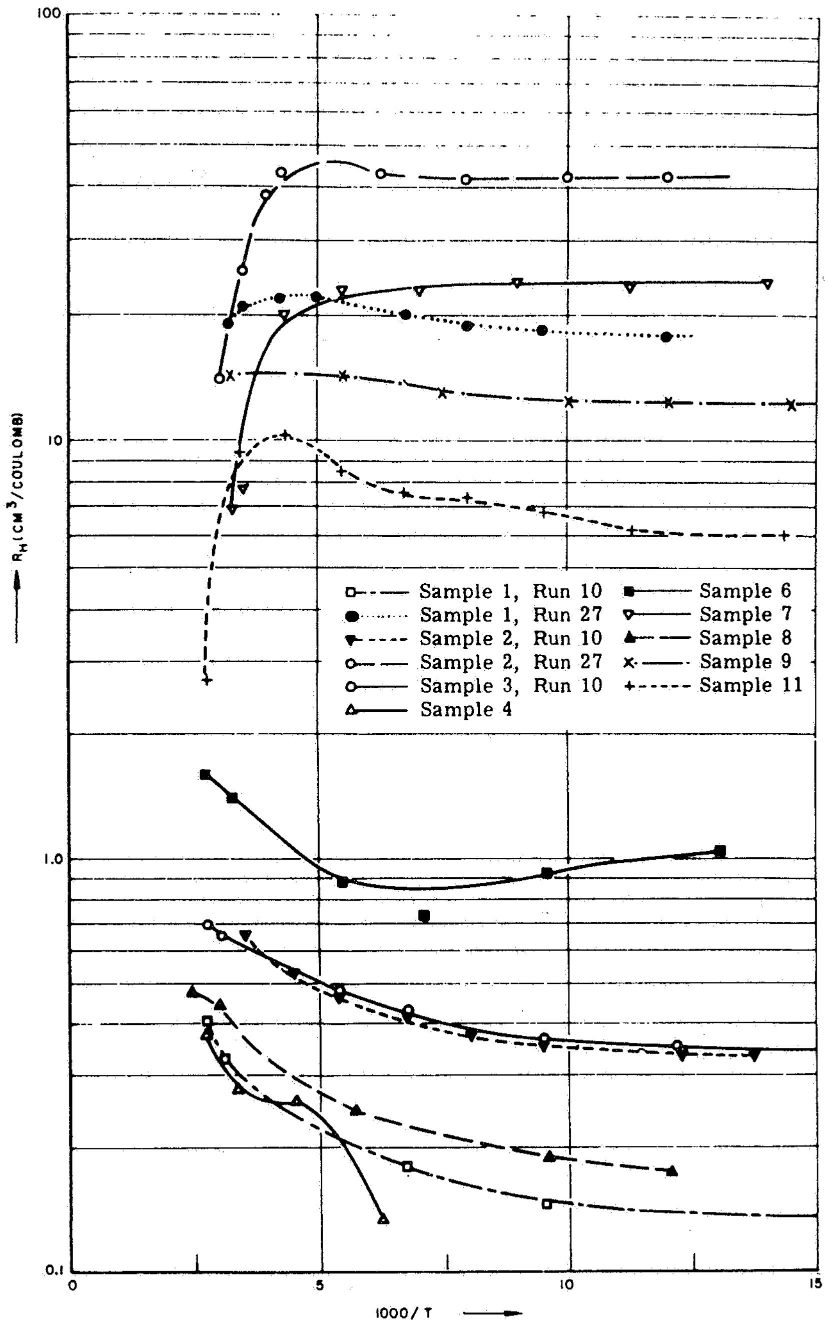


Figure 44. Hall Coefficient as a Function of Temperature for $Pb_{0.8}Sn_{0.2}Te$

As shown in Figure 44, for unannealed samples the Hall coefficient remains constant at low temperatures and rises steadily as the temperature is increased. For annealed samples, whose carrier concentration is about two orders of magnitude less, the increase in Hall coefficient at higher temperatures is small (and in some cases non-detectable) and is followed by a sharp decline until the sample becomes n-type. If we assume that the carrier mobilities are not too different, intrinsic condition is reached when R_H is also applicable to lead salt alloys. It is a good guess that if the as-grown samples are heated to higher temperatures, R_H would exhibit a maximum following which intrinsic conduction would dominate. The rise in R_H can be explained either by assuming a non-parabolic, non-ellipsoidal one band model or by assuming a two-valance-band model. The fact that the change in R_H is higher for higher concentration samples seems to favor the two-band model. The pertinent equations for this case are:

$$R_H = \frac{r}{e} \frac{p_1 b^2 + p_2}{(p_1 b + p_2)^2} \tag{1}$$

$$\frac{p_1}{p_2} = \left(\frac{m_1^*}{m_2^*}\right)^{3/2} e^{\Delta E/kT} \tag{2}$$

$$p_1 + p_2 = N_A - N_D = \frac{r}{eR_o} \tag{3}$$

$$\frac{R_H - R_o}{R_o} \approx \left(1 - \frac{1}{b}\right)^2 \left(\frac{m_2^*}{m_1^*}\right)^{3/2} e^{-\Delta E/kT} \tag{4}$$

$$\approx \text{const.}\ e^{-\Delta E/kT} \tag{5}$$

where p_1, p_2 are the hole densities in the two bands separated by energy ΔE. R_o is the Hall coefficient at low temperatures, r is the Hall constant, b is the ratio of carrier mobilities, m_1^* and m_2^* their effective masses and e is the electronic charge. Results for Sample A-1 are plotted in Figure 45 where $\ell n\ (R_H - R_o/R_o)$ is plotted against $1/T$. The data points fall on a straight line indicating that equation (5) is reasonably well satisfied. From this we calculate $\Delta E = 0.04$ eV which does not seem unreasonable.

A few samples were cooled to 14°K with no significant change between 14°K and 77°K. Further, no large dependence of Hall data on magnetic field strength was observed.

Hall measurements on vapor-grown crystals show the carrier concentration in the as-grown state is about an order of magnitude less than that in Bridgman grown crystals. This encouraging result, coupled with the fact

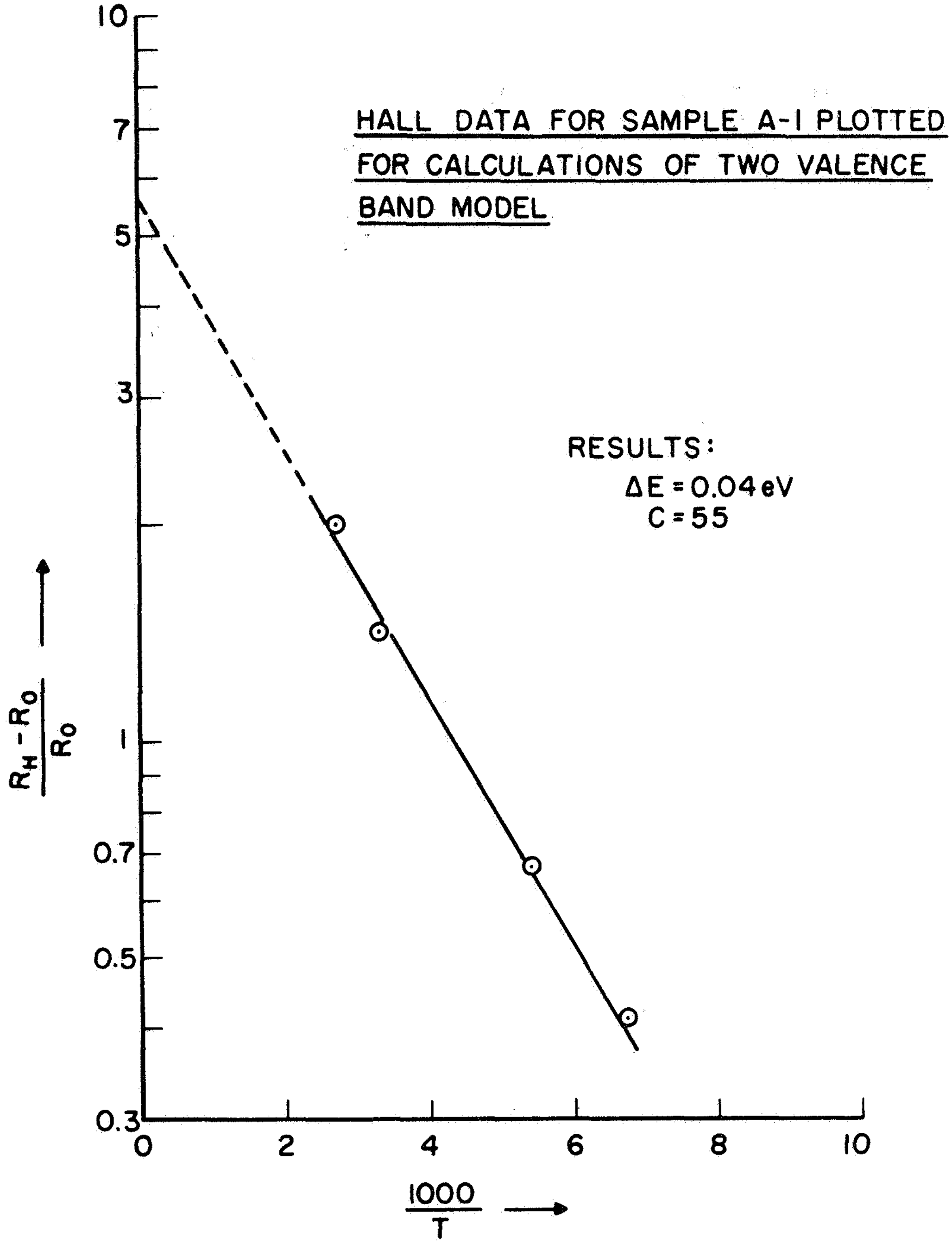


Figure 45. Hall Data for Sample A-1 Plotted for Calculations of Two Valence Band Model

that we can grow reasonably large crystals by the vapor growth method has persuaded us to devote more attention to this method of growth.

Figure 46 shows Hall mobility as a function of temperature for several single crystal $Pb_{1-x}Sn_xTe$ samples. At liquid nitrogen temperature, mobilities up to 20,000 cm^2/volt sec have been achieved in annealed samples. In this temperature range $\mu \sim T^{-2.0 \text{ to } 2.5}$ indicating that the dominant scattering mechanism is lattice phonons, which is also the case for PbTe. However, in order to be certain, the temperature dependence of effective masses must be investigated. At 82°K, μ is also a function of carrier concentration; decreasing by about 20 as the concentration increases from $3 \times 10^{17}/cm^3$ to $3 \times 10^{19}/cm^3$, in qualitative agreement with the Conwell-Weisskopf formula.

To sum up, Hall measurements on several $Pb_{1-x}Sn_xTe$ samples show that in the as-grown material, carrier concentrations are high ($\sim 10^{19}/cm^3$) and mobilities low ($\sim$500 cm^2/volt sec). For device work, particularly as an infrared photoconductor, this material is of no use. Hence it is essential that these material properties be improved. This has been done by vapor equilibration technique, details of which are described in the next section. The results we have obtained show carrier concentration about $10^{17}/cm^3$ and mobility about 15,000 cm^2/volt sec at 82°K. These values are satisfactory for photovoltaic detector fabrication. By annealing for longer periods, Harman has obtained concentration around $3 \times 10^{15}/cm^3$ and was able to observe photoconductive response in the 8 μ - 14 μ region.[12]

For the sake of completeness we mention our work on thin film $Pb_{0.8}Sn_{0.2}Te$. Thin films of $Pb_{1-x}Sn_xTe$ were deposited on pyrex, NaCl and KCl substrates at 10^{-6} torr from a single source material. A conductor pattern was registered on the pyrex substrate by conventional photolithographic techniques. The thickness varied from 1500 Å to 5000 Å. Optical absorption tests on these films show that the absorption starts to fall off in the 7μ - 8μ region. In some cases, a change in the slope of the fall-off curve was observed, indicating a non-homogeneous film.

B. FABRICATION OF p-n JUNCTIONS OF $Pb_{0.8}Sn_{0.2}Te$

We have prepared p-n junctions of $Pb_{0.8}Sn_{0.2}Te$ by the isothermal annealing technique of Brebrick and Allgaier. It is well known that excess metal and excess non-metal defects introduce donor and acceptor levels, respectively, in $Pb_{1-x}Sn_xTe$. The concentration of these defects can be controlled by equilibrating the sample under isothermal conditions with an alloy powder of known composition outside of the solidus field. The Bridgman grown crystals with 20 mole % are p-type. Various annealing temperatures and times have been tried. Junction depths as large as 7 mils has been obtained after annealing for 53 days. Shallower junctions have been obtained in two days of annealing.

According to recent studies, the diffusion mechanism can be described by

$$\frac{C(x,t) - C_o}{C_s - C_o} = 1 - \frac{4}{\pi} e^{-\frac{\pi^2}{\ell^2} Dt} \sin \frac{\pi x}{\ell}$$

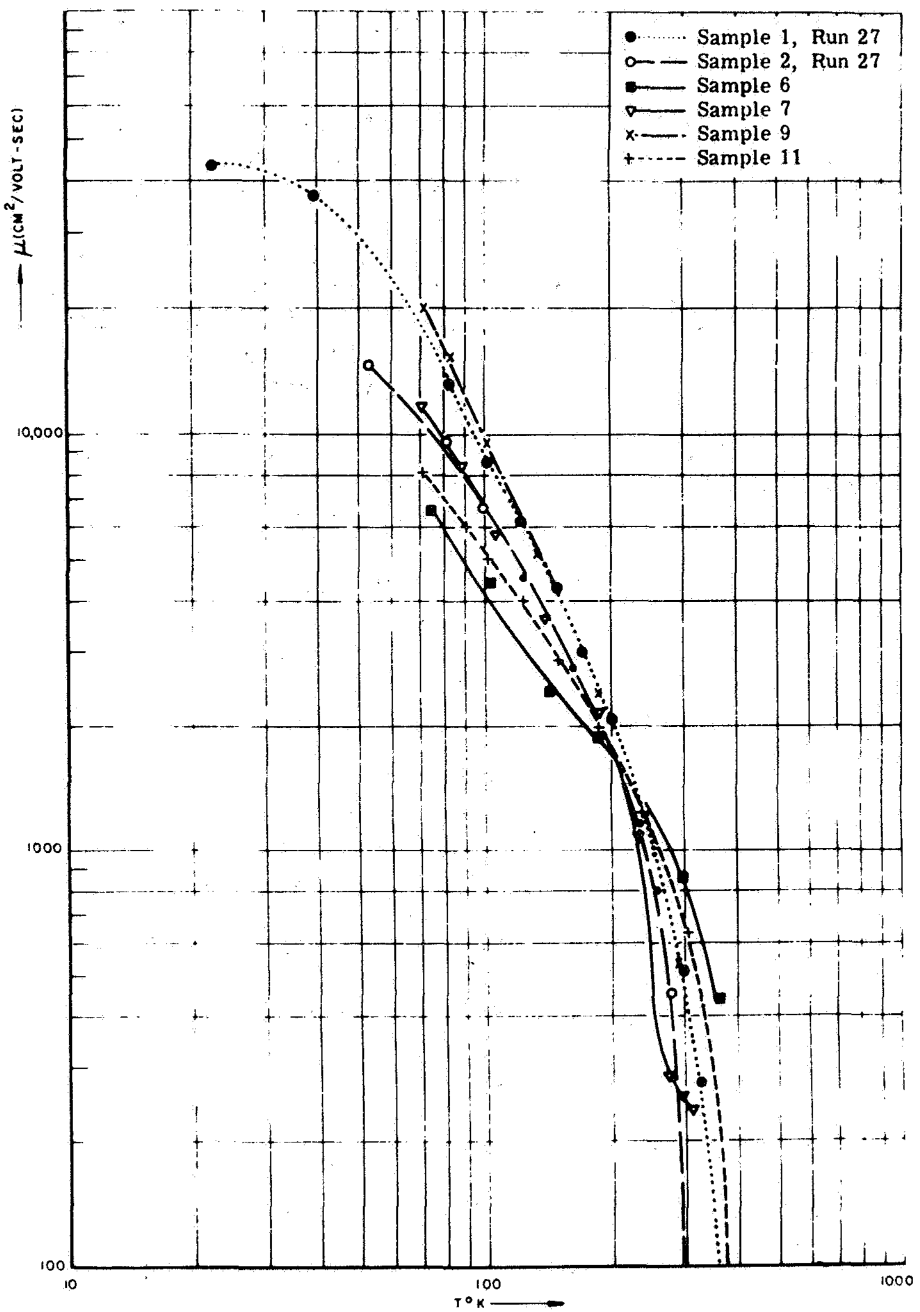


Figure 46. Mobility as a Function of Temperature for the Bridgman-grown Crystal (Sheet 1)

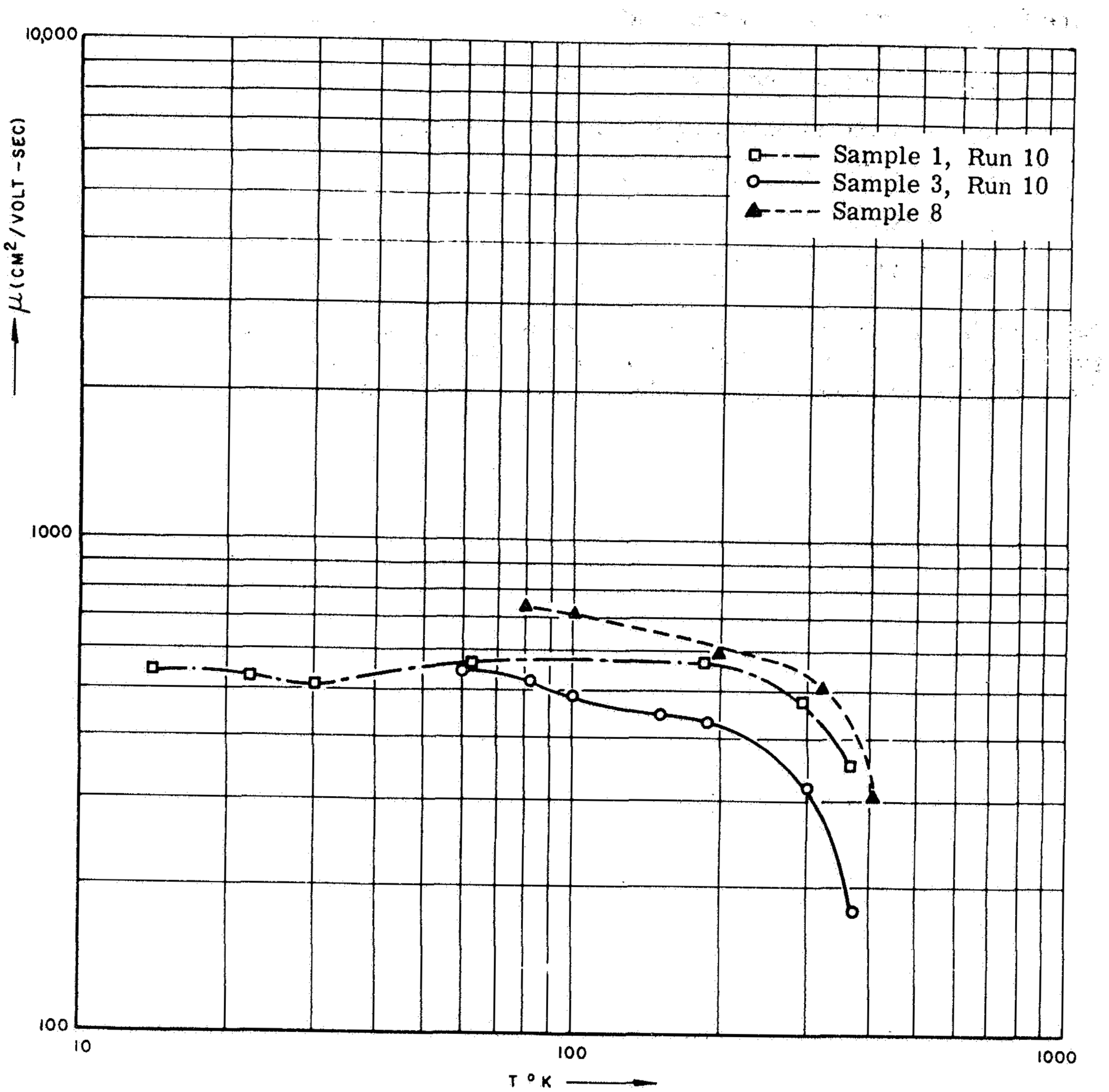


Figure 46. Mobility as a Function of Temperature for the Bridgman-grown Crystal (Sheet 2)

where C (x, t) = net concentration at a distance x from sample surface and

C_s = constant source concentration,

C_o = initial concentration in the material,

D = diffusion coefficient,

t = time,

ℓ = sample thickness.

The diffusion mechanism, however, is sensitive to surface condition and crystal defects, and deviations from equation 6 have been observed. Figure 47 gives a pictorial summary of the sequence of events involved.

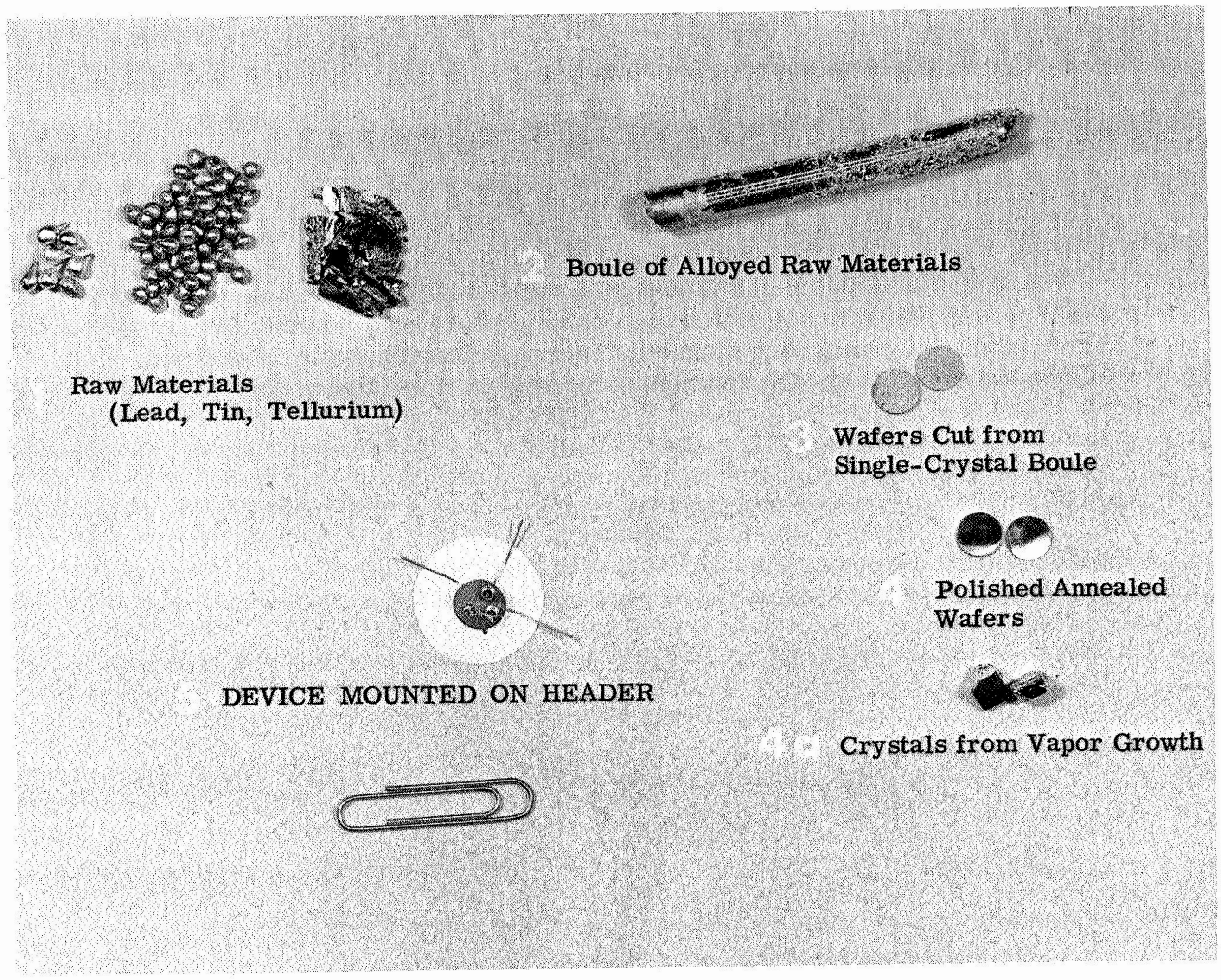


Figure 47. Sequence of Operations in Fabrication of $Pb_{0.8}Sn_{0.2}Te$ Detectors

IV. ELECTRONIC SCANNING AND READOUT

A. SYSTEM CONSIDERATIONS

The signal processing section of the image sensor array is designed with several primary goals centered around compatibility with the detector array in size, operating temperature, and detector characteristics. In addition, practical considerations are considered to realize a working model at an early point in time.

The overall system is shown in the system diagram of Figure 48. The system consists of the optical portion before the detectors, including the lens and chopper. Following the detectors are preamplifiers and scanning circuits, with the required supporting scan control circuits and output amplifier circuit. The final signal processing is performed external to the image sensor package, and determines the operating system bandwidth for each detector. The mode of operation for the external processing could be either a number of channels operating in parallel, or a single channel operating serially as shown in Figure 48.

The overall system performance is determined primarily by three factors, the D* of the detector, the noise of the preamplifier, and the system noise bandwidth. Since the latter is determined external to the scan system, it may be changed at will. The first two are primarily determined by a device (detectors in the array or transistors in the preamps) and how well they match each other. The goal of the system design is to achieve the match between the detector and preamp such that the effective D* of the system approaches the D* of the detector. In practice, the preamp adds a small amount of noise, and the system D* is slightly lower than the detector D*. The use of the charge storage scanning scheme, when used as shown in Figure 48, does not greatly alter the system bandwidth. The integration that takes place in the charge storage capacitors is periodically sampled at a rate that is greater than the useful system bandwidth; hence, these externally determined bandwidths mask the influence of the charge-storage scheme.

Some of these design goals proved to be somewhat limiting in implementation. For example, the complexity of the post scan processing is considerably more involved than the comparable pre-scan processing, the latter being primarily a consideration of gain and bandpass.

The original circuitry, constructed during Phase II of the program, was designed to be as simple as possible, in order to achieve minimum size and complexity. As a result, there is little chance to significantly increase its performance with simple modification. In particular, gain stability was shown to be even more necessary for usable system operation than originally predicted. It is possible to trade gain stability for gain by adjusting the feedback network; however, because of sampling noise, the lack of gain is an equally critical problem.

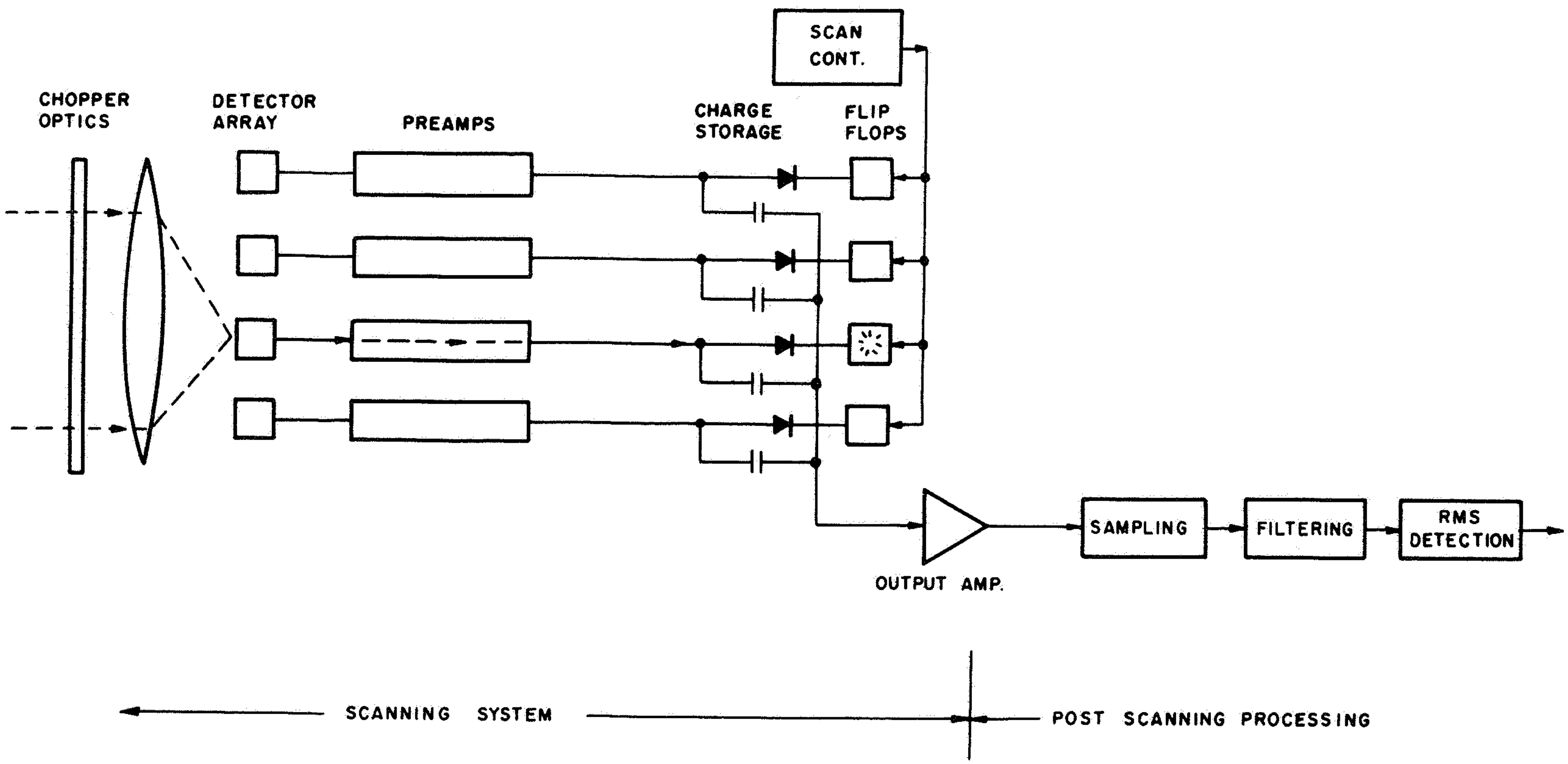


Figure 48. Operating System Diagram

The use of charge storage readout of the preamps as a scanning mechanism has some potential advantages; however, it may magnify other problems. In particular, the charge storage system is essentially an integrating scheme, and this type of response magnifies D. C. bias variations.

The commutation of a large number of low-level signals to a common bus can be accomplished with the scheme of Figure 48. One aspect of importance in commiting these very low level signals is the efficient use of the small amount of energy available.

Specifically, as the commutating system sequentially connects each output to only one source at a time, the signal at the multiplicity of unconnected outputs is essentially "wasted." The straightforward method around this problem is to add extra amplification ahead of the commutation process. The approach used in the charge-storage readout technique is to integrate this "wasted" signal and deliver it during the small readout time. Thus, an approximate "gain" is available in proportion to the "wasted" energy; i. e., the ratio of the sample repetition time to the sample time. This, of course, becomes significant only for a relatively large number of commutated segments.

With reference to Figure 48, the currents to be commutated from the low level collector circuits charge the commutating capacitors. The digital scan generators reverse-bias the switching diodes. The lower bound on the signal current is the leakage current of the switching diode. The rate of change of signal current should be limited to 1/2 the scan rate or less. As each scan pulse generator sequentially forward-biases the corresponding switching diode, a discharging current flows in the capacitor. Note that all capacitor ground returns flow through a common sensing point. This is detected by the output amplifier and constitutes the output signal. Thus, when used directly with very low leakage devices (compared to the signal currents), the charge-storage scheme has a considerable advantage. When a D. C. bias current forms a significant portion of the input to the charge storage mechanism, the output is extremely sensitive to these small output variations. Figure 49 shows the well known general frequency response of an integrating scheme that is responsible for this characteristic.

The sampling mechanism and physical circuit components limit the actual D. C. response in a non-linear manner. This is observed as a saturation effect in actual practice, and indefinitely large outputs do not occur. It is clear that the integrator should be maintained in its linear range throughout the active portion of the input cycle. The input of the integrator consists of a DC component and an AC component. The primary function of the DC is to bias the integrator operation to permit sampling with unidirectional sampling gates. This would not be a requirement of bidirectional circuitry, such as with MOS sampling devices, if such an output format were acceptable. The unidirectional output format is more convenient to use with video processing equipment without special modifications.

The AC operation is primarily determined by the desire to operate the preamplifiers with much lower signals than is possible in the DC mode of operation. Typically, the operation is limited, in the DC mode, to the order of millivolts (the DC offset voltage) and in the AC mode at least three orders

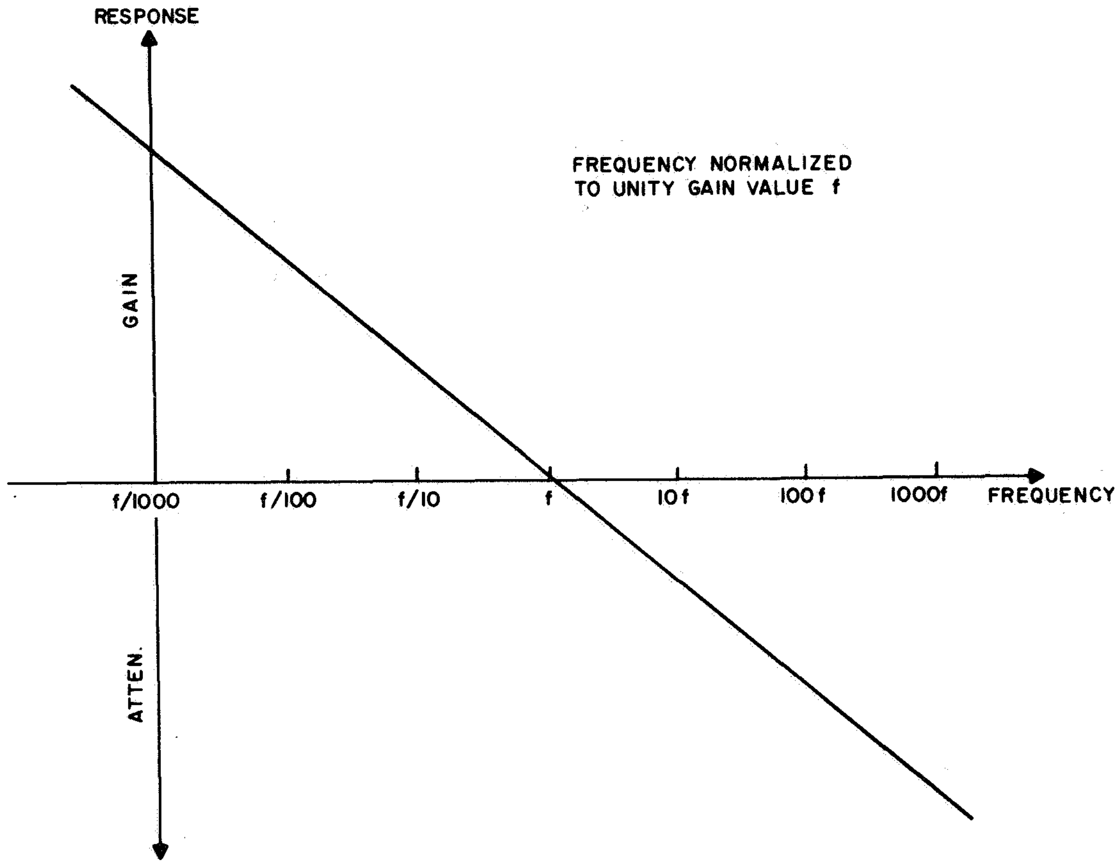


Figure 49. Frequency Response of Integrating Scheme

of magnitude less, depending on the bandwidth, and stray pickup. Thus, it is desirable to operate in an AC mode from a signal-level point of view, in order to approach the detector noise limit in sensitivity. The overall system can operate with A-C coupled amplifiers and give an apparent DC response if the optical chopper is operated in synchronism with the scanning. Essentially, the scanning operation can provide the function of synchronous demodulations, which can exhibit an overall DC transfer function (optical input to synchronous demodulator output). Not all systems require DC response, however, and some applications require emphasis on the changes in IR image detail. Thus, an A-C coupled system performs this function inherently, if no optical chopper (modulator) is employed. The output scanning then loses its ability to provide synchronous detection. However, since the output must be scanned, it will have a regular periodicity.

No special requirements are imposed on the preamplifier circuits for producing an image from the line-scan array. The primary difference in operation concerns scanning the input image optically and simultaneously presenting the output in a corresponding scanned format. The bandwidth of the preamplifier circuits limits the scan rate or resolution unit time in the optically scanned direction. Similarly, the low-frequency preamplifier cut-off will determine the discrimination characteristic of the unchopped optical input signal.

B. PREAMPLIFIER REQUIREMENTS

The preamplifier requirements for the line-scanned image sensor have several conflicting criteria. They should be small to eliminate fan-in of wiring, preferrably at the density of the detector elements. They should be simple to achieve the above requirement and to permit fabrication in mass form; they need high power gain to permit a fairly large amount of negative feedback and to interface the detectors and a fairly large impedance ratio from input to output.

The preamp has three major functions to perform; (1) stabilize the detector bias (2) impedance matching, and (3) power gain. The first consideration of stabilizing the detector bias is a result of using the charge storage technique. The voltage on the charge storage capacitor varies as a function of the incident radiation, integration time, etc. The detector voltage-current characteristic is sensitive to such variations and causes major changes in the performance of the detector. Isolating the detector from the charge storage capacitor with a preamplifier then allows an independent choice of the optimum detector bias.

The function of impedance matching is the second critical attribute of the preamp. The detector-charge storage combination could give useful results only if an impedance matching transformer were connected between the two. Typically, a transformer with an input impedance of 10^5 ohm and an output impedance of greater than 10^9 ohms would be needed to produce the required match. The desire to use micro-components, and the unreasonably large numbers quoted above, are two reasons this scheme can not be used. Ultimately, it would be desirable to develop a detector with greater than 10^9 ohms; however, for the present, the preamp will have to perform this function. The choice of input impedance could be made to optimize this impedance with respect to noise, power transfer, or detector performance. In general, these requirements conflict, and a compromise will have to be reached which also considers the range of values obtainable with preamp input components. Impedance matching with respect to noise will produce the best system D* and is a prime consideration. Impedance matching with respect to maximum power transfer will result in the lowest required power gain of the preamp and, hence, the fewest components. However, as a first-order approximation, it is not expected that this optimum impedance value will be significantly more efficient than the value chosen for the best noise characteristics. The third choice of preamp input impedance would consider the detector performance. If the detector is operated into a load impedance much lower than the detector impedance, a current flow proportional to the photon input will flow. If the detector is operated into a load impedance much greater than the detector impedance, an output voltage will be developed which approximates the logarithm of the photon input. Intermediate values of impedance will then give a combination of the two responses.

The final purpose of the preamp of providing useful power gain will be important only to the extent that the impedance matching gives an inefficient power transfer. This is because a large gain is already available in the charge storage mechanism. To arrive at a minimum preamp, it is necessary to compromise output impedance for more power gain.

C. MULTIPLEXER REQUIREMENTS

The multiplexing mechanism is a key focal point in design consideration. The design of the preamp essentially revolves about interfacing the detector to the multiplexer circuitry. In the ideal case, no preamp is required and the multiplexer is directly connected to the detector array. In a sense, the purpose of the preamp is to "make up" for the deficiencies of the multiplexer. Three parameters are critical to the multiplexer: (1) sensitivity, (2) speed, and (3) fan-in (switch ratio and stray coupling).

The sensitivity of the multiplexer directly relates to the size of the preamplifier. Conversely, if the preamplifier is fixed, it relates to the limiting system sensitivity. It is, of course, strongly influenced by the speed, and fan-in requirements. Thus, polycrystalline photoconductors have been successfully used in commercial equipment to switch one microvolt level signal in a few tens of cycles per second. In the present system, it is desired to switch 50 signals at sub-milli-second speeds. The available devices force several millivolt signal levels for output multiplexing, This, in turn, dictates larger preamps.

D. CIRCUIT IMPLEMENTATION

In summary, the design goals of the preamp are (1) ultimate integration, (2) minimum size/component count per preamp, (3) low noise figure, (4) low temperature operation, and (5) matched system impedance.

Three basic circuit types are available for the basic circuit design. The most straight-forward would be the AC coupled preamp with all elements operating independently at its own optimum bias. The goal of ultimate integration negates this as a practical solution, since capacitors and transformers are required to effect the AC coupling. The second amplifier type would be a direct coupled differential amplifier. This type of design requires carefully matched components to achieve high gain with few components. In this respect, integrated circuits stand out as one method of achieving this desired match between components. The third type of circuit would use complimentary transistors to allow DC negative feedback for bias stabilization. This is probably a more desirable form of bias stabilization as contrasted with the differential case where the degree of balance is required to control the saturating or cutting off of an advanced amplifier stage. This is particularly likely when high voltage gains are to be realized to achieve the type of impedance match required here.

The choice of the preamp input device is intimately connected with the overall system concept. In light of the previously stated preamp design goals we will consider the properties of the various input devices. The MOS-FET (Metal On Semiconductor Field Effect Transistor) is currently not a strong contender because of its high noise characteristics. The junction FET has the advantages of very low noise. It will operate at low temperatures and in fact its performance peaks around 77°K. It has a simpler manufacturing process than bipolar transistors. The disadvantages of the J-FET are that it must operate at a high input impedance to realize the full benefit of its low noise characteristics. It dissipates a large amount of power, and in fact, the higher performance devices may be distinguished in general, by the higher currents drawn at zero gate to source voltage. Hence, a number of the devices would substantially increase the heat load of the array cooling mechanism. Finally, J-FET's are 3 to 5 times the size of comparable bipolar transistors.

The contrasting views for bipolar transistors offer the following advantages. The bipolar transistors are at a more advanced level of technology particularly in integrated arrays. They occupy 1/3 to 1/5 the area of J-FETS. They can have a low noise at some impedance level, and this usually matches the detector impedance reasonably well. Bipolar transistors can operate with 1/10 to 1/100 of the current at which a J-FET operates and has a corresponding lower power dissipation. On the disadvantage side, bipolar transistors can not operate at low temperatures. The useful β of these devices are usually specified by manufacturers only as low as -55°C. Thus their use would require construction of a thermal drop from the preamp to the detector array. However, the differences in physical sizes will dictate such a structure any way. Thus, this is not a serious immediate consideration. The bipolar transistor also requires a more involved structure than J-FET's to achieve isolation in the monolithic form.

The detector array diodes require the high impedance input of the FET and ac coupled stage, implemented on a separate circuit board near the detector array. The high impedance circuits are very susceptible to stray electrostatic pickup; thus, it is imperative to minimize the interconnecting lead between the FET and the detector diode. The minimum length is essentially limited by a combination of the fan-out and connector configuration. The circuit diagram of this intermediate circuit board is shown in Figure 50. Each circuit consists of a source follower FET circuit with a direct-coupled input and an ac coupled output. The input impedance will be very high ($10^8\Omega$). The output impedance will approximate $1/g_m$, for the FET, or in the neighborhood of 1 kilohm. Thus, pickup in the output leads will be negligible. The double resistor output network is necessary to maintain the input bias condition for the present circuit boards. Also, the inherent feedback of the source follower circuit will give a uniform gain characteristic for all these (≈ 1).

The modifications to the amplifier/scan circuit boards built under the previous contract are shown in Figure 51; note the ac feedback network of the 2.2 μfd capacitor and the 5K resistor. The bias of the NPN transistor pair has been reduced to get better control of the steady-state charging current of the charge storage capacitor (the 10 megohm and the 2.4 megohm resistors). Because of the tolerance of the charge storage capacitor (50 vpf) (5%), the steady-state output will still vary 5%.

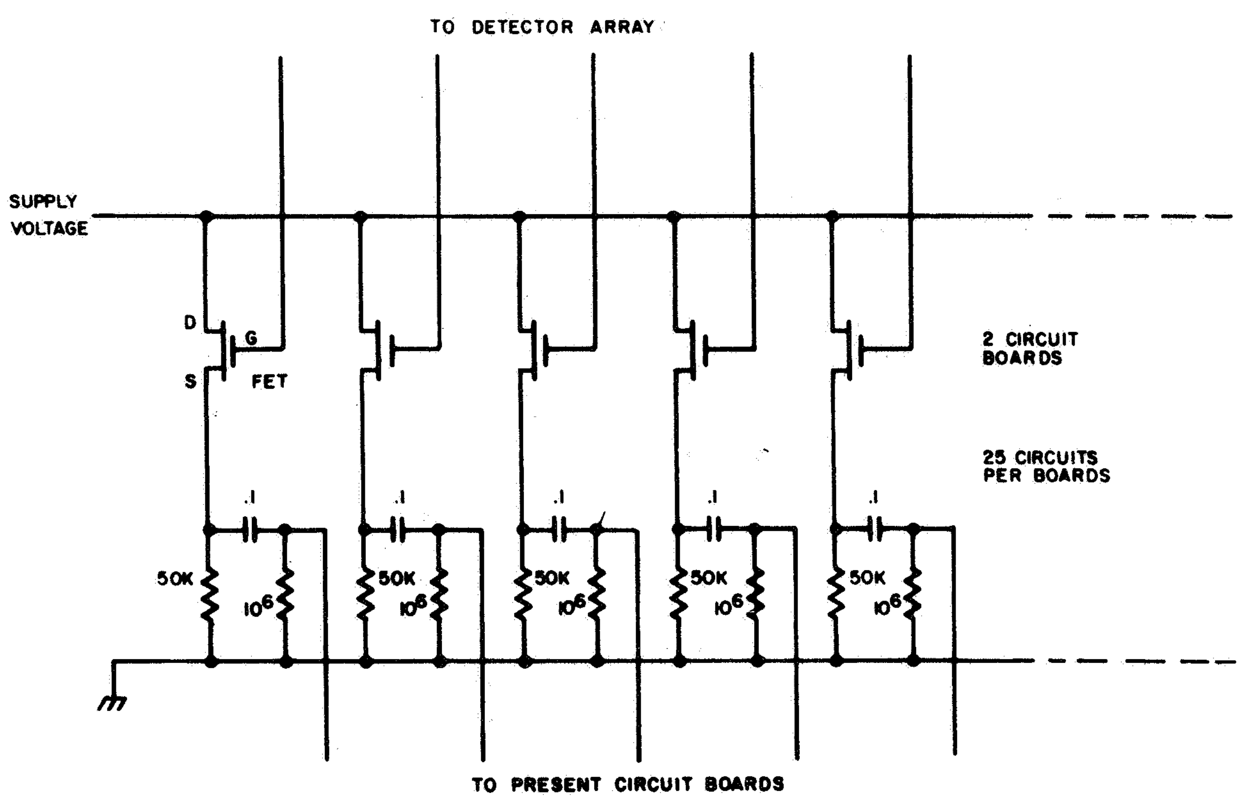


Figure 50. FET Input Circuit Boards

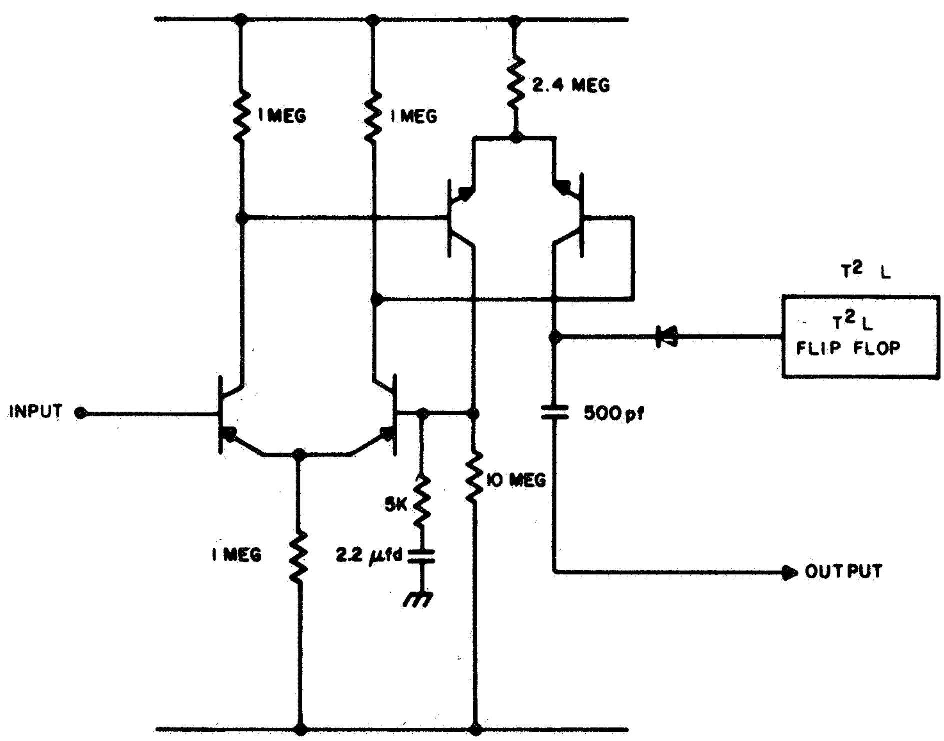


Figure 51. Modified Feedback Network on Present Amplifier

Because of the problems of the minimum component circuit described, the design was reconsidered in light of commercially available amplifier devices.

Some tests were made with silicon monolithic operational amplifiers. Of the best available today, several features are not adequate for direct use. From Figure 52, it is apparent that a considerable number of external components are required to implement a detector preamplifier system using these units. First, the input impedance is too low and an external FET input circuit is required. The amplifier must contain some form of compensation (the 30 vpf capacitor) to make it stable. This compensation circuit can be used to further limit the band-pass if desired. The feedback network must provide for dc stability because of the high open-loop gains available ($> 10^5$). The output can swing into saturation, due to a small temperature differential on the silicon chip. Finally, the output is low impedance and not directly compatible with the charge storage sampling scheme.

On the positive side, several important features make the operational amplifiers attractive. First, they represent the first step toward miniaturization of the amplifier. The required outboard components are available in hybrid form; in fact, several manufacturers specialize in hybrid assemblies consisting of FET input stages, compensation, and a monolithic operational amplifier chip. The use of an MOS-FET analog output offers some advantages in the power level at which sampling can take place. As an example, consider the signal power in a charge storage scheme, the values being determined by the components available.

$$P = E \times I$$

$$P = (1) \times (10^{-6}) = 10^{-6} \text{ watts}$$

Now, consider the signal power in a low-level MOS sampling scheme.

$$P = \frac{E^2}{R}$$

$$P = \frac{(0.01)^2}{10^6} = 10^{-10} \text{ watts}$$

The charge storage scheme has been operated near this power level with silicon photodiodes; however, this type of operation is not possible with a transistor amplifier (FET or bipolar) because the leakage currents are too high and the transfer gains too low for operation in this range. Thus, there appears to be a lower amount of preamplifier gain required in the MOS sampling system. This would be manifested as more negative feedback to provide tighter gain control (uniformity) in the preamplifiers. This is another advantage of the operational amplifier over the discrete amplifiers available; the operational amplifiers have more stages and, hence, higher open-loop gain permitting tighter gain control than the other amplifiers. Although the present trade-offs are about a "draw," it is anticipated that monolithic amplifier structures will be readily available in the near future to perform the preamplifier functions.

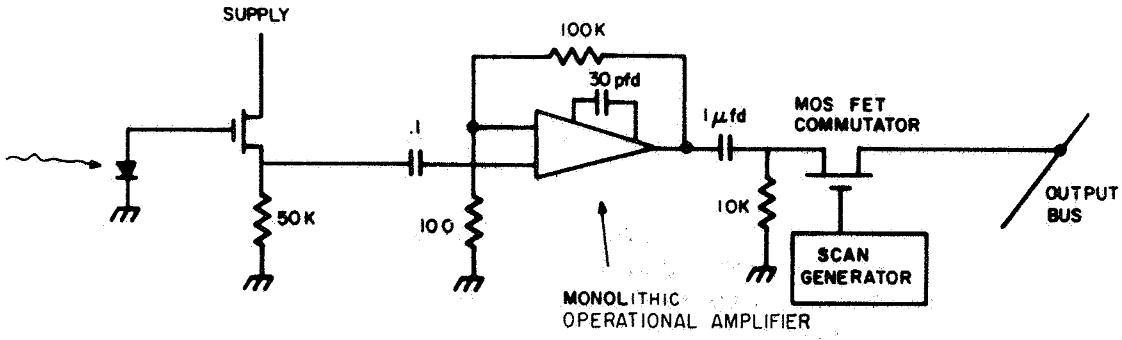


Figure 52. Hybrid Amplifier System

V. ASSEMBLED MODEL

The scanned detector system assembled during this phase of the contract consists of the basic assembly described in the Phase II Technical Report, plus the modifications incorporated into the design during Phase III. The complete assembly is shown in Figure 53. In particular, modifications were made to the optics, dewar, and preamps.

A. DETECTOR PACKAGING

The scanned detector assembly is designed about the molded plastic block containing the diode array. This block functions as an integral part of the demountable vacuum system in which the array is enclosed. The block, shown in Figure 54, consists of the main body, which incorporates the vacuum feedthrough connections and the detector mounting board that contains the array, a fanout lead pattern, and a "cold finger" for connection to the cooling system. Electrical connections from the array to the fanout pattern are shown in Figure 55. The two components in Figure 54 are mated together such that the fanout lead pattern matches the vacuum feedthrough pattern, and the cold finger extends through the back surface of the block. The assemblies are then bonded to be vacuum tight. The overall dimensions of the block are 2.5" × 3.5" × 5/8" thick.

B. COOLING

The InAs array operates at any temperature from 300°K down, with an increase in sensitivity as the detector is cooled. The model assembled for this program consists of a simple foam insulated container that makes thermal contact with the "cold finger" from the array package. When filled with liquid nitrogen, the array is cooled to a temperature of -125°C. Lower temperature could be achieved by enlarging the thermal contact area between the cold finger and dewar.

The dewar and attached array block is shown in Figure 56. The dewar has a volume of 11 cubic inches and maintains the array below -100°C for 15 minutes after filling.

C. OPTICS

The optical train was designed to operate with an optical chopper as an integral element. To minimize the required chopper opening, the chopper is placed at the image plane of the objective lens. A relay lens is then used to image the chopped scene onto the detector array.

The lenses used are made from Type 125 quartz, having an average transmission greater than 90% over the spectral band 0.26 to 3.3 μ. The index of refraction varies uniformly in the spectrum of interest from 1.40 at 3.6 μ to 1.45 at 1.0μ. The objective lens is f/5 1" diameter and the relay lens is f/1 1" diameter.

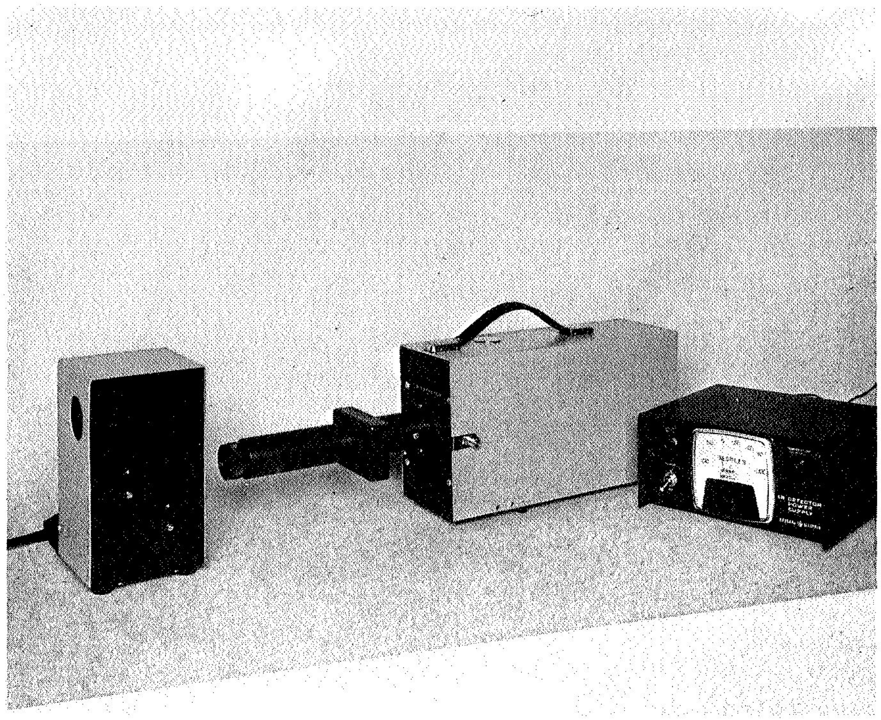


Figure 53. IR Detector System

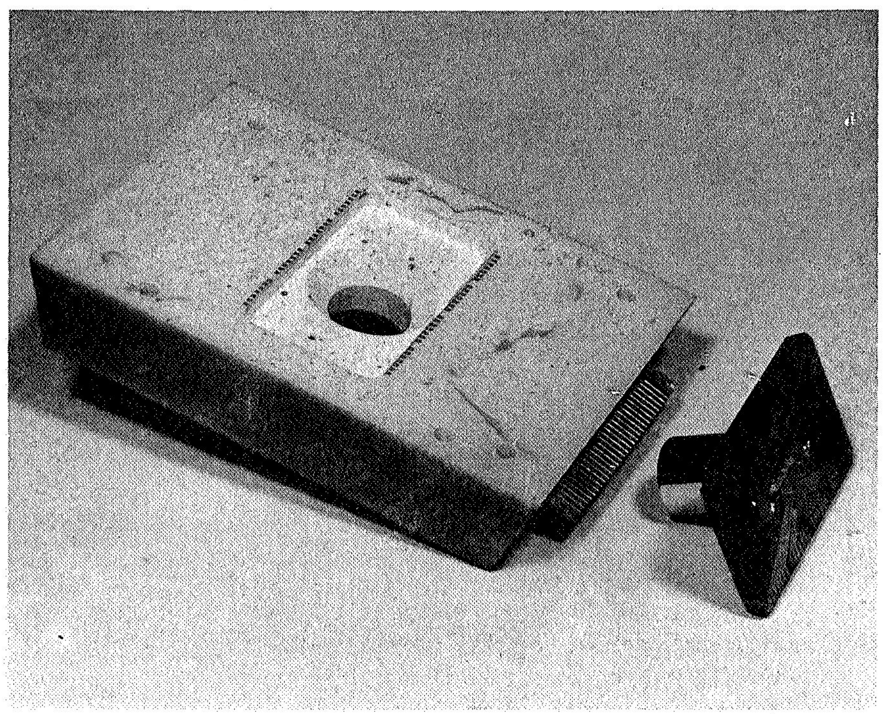


Figure 54. Mounting Assembly

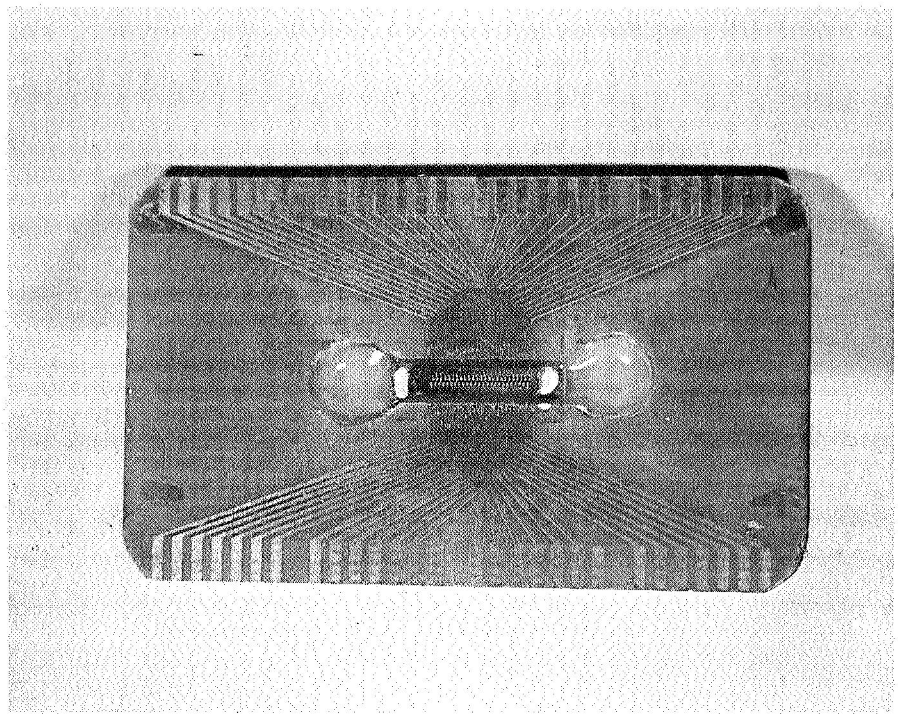


Figure 55. Electrical Connection from Array to Fanout Pattern

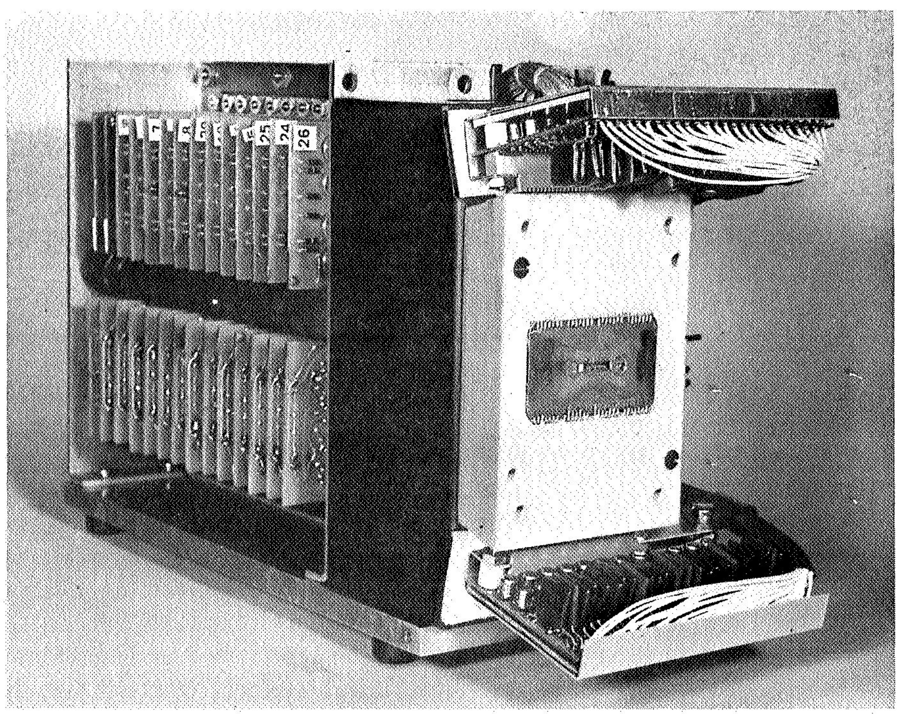


Figure 56. View of Array Block and Driver

The assembly is shown in Figure 57. The fixture mounted to the plastic block forms a vacuum chamber to prevent frost formation on the detector chip. A silicone rubber o-ring seals the fixture to the plastic surface, while the relay lens forms the second seal to the vacuum chamber. The field lens is at the opposite end of the focus tube and is adjustable tofocus on sources from 12 inches to infinity.

The chopper is a driven tuning fork assembly mounted in a housing along the focus tube. The chopper blades are 0.95" long and open to a maximum slit of 0.04 inch. Since the detectors are completely illuminated as soon as the slit is 0.019", a near-symmetrical modulation is achieved. The chopper operates at 800 cps.

D. PRE-AMP PACKAGING

As described in Section IV, the preamplifier circuits were modified to include AC feedback and an FET input. The AC feedback was easily incorporated onto the same plug-in boards, shown in Figure 57 to the rear of the dewar. The FET input, however, should optionally be placed as close to the detector element as possible, so as to minimize pickup.

The most convenient location for the FET circuit is immediately after the printed circuit board feedthrough on the molded block. The FET, along with bias resistors and coupling capacitors, are assembled onto a small printed circuit that plugs into the array module block. The output of this circuit is of relatively low impedance and can thus be directly wired, via cable, to the preamp cards.

The logic and control circuitry to drive the chopper and sequence the amplifier outputs remain unchanged from the previous program. It is housed in the auxiliary control box shown in Figure 53.

E. TEST TARGET

To demonstrate the capability of the array in imaging sensing applications, a test target and image scanning device was assembled.

The test target consisted of a uniformly heated gray surface. Output of the surface is calibrated with a point detector and compared with a blackbody at equal temperature. Pattern generation is achieved by placing a patterned aperture plate a short distance in front of the surface, creating a non-gray-scale image. Black and white levels are controlled by the temperature of the source and the aperture plate.

Scanning of the target is accomplished with a rotating mirror assembly, shown in Figure 53. The mirror rotates at a speed that enables the electronically scanned horizontal line to be traced out several times as the vertical position moves through one resolution line. The scanner is electrically coupled into drive circuitry such that the output signals driving the display scope trace a frame in synchronism with the mirror.

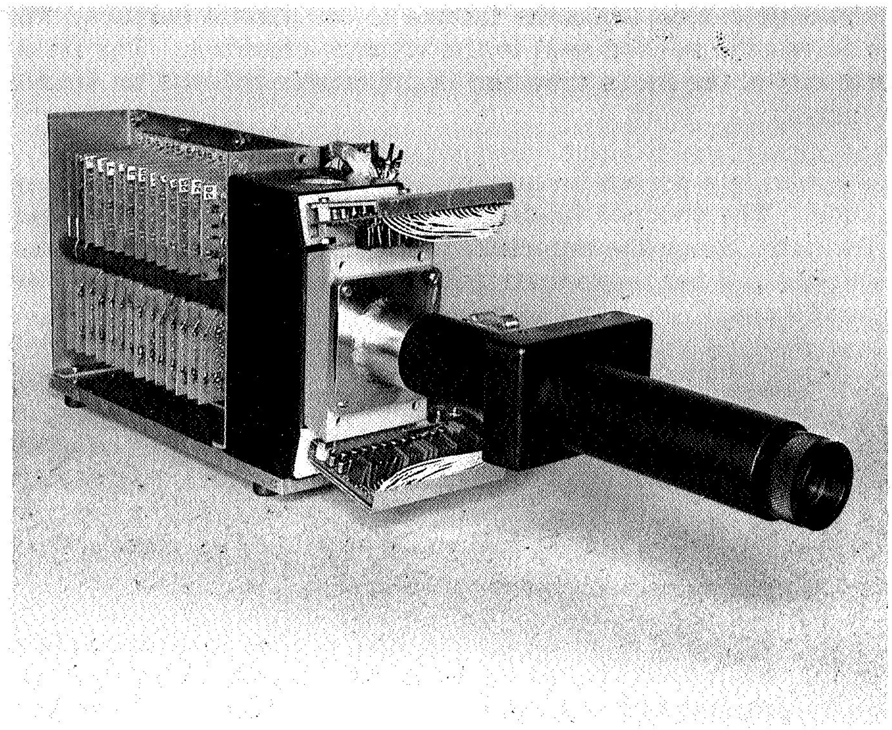


Figure 57. Lens Assembly Attached to Array.

V. RECOMMENDATIONS

The intent of this program was two-fold: (1) to determine the ability to fabricate high-sensitivity InAs photodetectors in a monolithic form, and (2) determine the potential of achieving uniform arrays of these high-sensitivity elements. The results achieved during the program indicate that the work should be continued to the next stage of development, namely a manufacturing methods program whereby the laboratory techniques established by this program are transferred into a pilot line process.

The purpose of such a program would be to provide that type of process control which can be arrived at only by processing relatively large numbers of wafers with a totally constant environment. From such efforts, specific data on wafer yield and array costs can be accurately determined.

The study carried out on PbSnTe during the past two years indicates that the initial selection of this long-wavelength detector material was correct. Continuing advances in the material properties and the device properties have advanced this detector to the stage where an array development program can be reasonably initiated. Coupled with continuing programs for material and device optimization, electronically scanned linear arrays could be demonstrated in the very near future.

NEW TECHNOLOGY APPENDIX